Supplement for
HE800HSC600 and HE800HSC601

SmartStack ä
High Speed Counter Options

22 April 2004

SUP0265-04

PREFACE

This manual explains how to configure the High Speed Counter SmartStack Module.

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ABOUT PROGRAMMING EXAMPLES

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Note: The programming examples shown in this manual are for illustrative purposes only. Proper machine operation is the sole responsibility of the system integrator.

Revisions to this Manual

This version (SUP0265-04) of the SmartStack High Speed Counter Options User Manual contains the following revisions, additions, and deletions:

1. Revised register descriptions in Table 4.3 (Option 2).

2. Revised register descriptions in Table 4.5 (Option 2).

TABLE OF CONTENTS

USER FRIENDLY TIP FOR USING THE HSC600 / 601 SUPPLEMENT

In many instances, the user needs to only use **three** chapters in the *SmartStack ä High Speed Counter Options Supplement* for the HSC600 / 601:

1. Chapter 1 - lists the six options that are available.

2. Chapter 2 - provides initial configuration procedures (using Cscape Software) that leads the user to the Options Screen.

3. Upon selecting an option, consult the Table of Contents to determine which chapter the option is located in. **Each option has its own dedicated chapter and covers items such as:**

a. Functions and capabilities; pin-out
b. Registers
c. I/O Map - shows functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.
d. Configuration procedures
e. Advanced Use-Cscape Override Configuration Procedures – used only for applications needing to override the Cscape setup during runtime. Not used in most applications.

CHAPTER 1: INTRODUCTION

1.1 Scope

The supplement for the SmartStack™ High Speed Counter Options covers the six functional options of the HE800HSC600 / HE800HSC601 (HSC600 / HSC601) and provides configuration procedures using Cscape Software. Chapter One provides general information, and Chapter Two covers the initial configuration procedures that must be performed to select an option. The remaining chapters provide operational information and configuration procedures that are specific to each option. Each option has its own dedicated chapter.

1.2 Options Table

Table 1.1 lists the six options that the HSC600/HSC601 can be configured to function as:

Table 1.1 – Options for HSC600 and HSC601

Option #	Description
1	Dual 32-Bit Totalizer/Frequency Counter plus Dual 16-bit PWM/Pulse Outputs
2	Dual 32-Bit Counter with Output Latch, Pre-load Register and Two ON and OFF Comparison Outputs per Counter.
3	24-bit Electronic Cam with 8 Combinable ON and OFF Functions.
4	Dual 16-Bit Electronic Cams with 4 Combinable ON and OFF Functions per Cam.
5	Field Installable Option. (Cscape uses an external file to specify the counter function.)
6	Diagnostic Tool Option. (This option Is intended for hardware testing only.)

1.3 Configuration Overview (All Options)

The SmartStack™ High Speed Counter (HSC600/HSC601) offers a wide range of functional options for a variety of applications. One of six options is selectable during the configuration process using Cscape Software. The option selected determines the types of functions that the HSC can be configured for.

Upon choosing an option, additional selections are required to further define how the HSC600/601 functions. Using the Cscape Configuration screen, the user sets input and output parameters as well as other types of variables depending upon the option selected.

1.3.1 Advanced Use – Cscape Override Procedures

Note: The Cscape Override procedures are <u>not</u> intended for most applications and are recommended only for applications that require parameter changes during runtime.

Most application requirements are met using the standard Cscape configuration procedures described for each option in corresponding chapters throughout the supplement. The Cscape parameters remain the same (or are static) during runtime. However, there are some applications where it may be necessary to override the Cscape setup during runtime. Such applications are dynamic in that the parameters are changed while the program is executing. The HSC600/601 gives the user the flexibility of writing a ladder code program to allow a change to the Cscape parameters during runtime. Cscape Override configuration procedures are available for several of the six options and are located at the end of each applicable option chapter.

Note: Even if the user intends to change only one register using Cscape Override Procedures, then ALL registers must be configured from the ladder code as specified in the Cscape Override section for that option.

1.4 Before Getting Started

a. Wiring diagrams, specifications, and other pertinent information for the HSC600/601 are covered in individual data sheets created for each SmartStack Module. The SmartStack Module Supplement (SUP0246) contains all of the data sheets and is periodically revised to reflect updates and changes.

b. Installation and configuration procedures that are common to all SmartStack Modules are contained in the Control Station Hardware Manual (MAN0227).

1.5 Safety Warning (All Options)

Warning: Failure to disable the High Speed Counter Module (HSC600/601) manually through the ladder code program could cause either personal injury or damage to equipment.

When the OCS/RCS is in the Idle or Stop modes, the HSC600/601 continues normal operation. **The user must physically disable the HSC600/601 through the ladder code program.**

CHAPTER 2: INITIAL CONFIGURATION

2.1 Safety Warning

Warning: Failure to disable the High Speed Counter Module (HSC600/601) manually through the ladder code program could cause either personal injury or damage to equipment.

When the OCS/RCS is in the Idle or Stop modes, the HSC600/601 continues normal operation. **The user must physically disable the HSC600/601 through the ladder code program.**

2.2 Preliminary Configuration Procedures (All Options)

The following procedures are used to select one of the six options. After an option is selected, read the chapter that is dedicated to the particular option. Each option chapter provides operational information and additional configuration procedures.

The SmartStack configuration is accomplished through the Configure Controller Type Dialog.

1. From the Main Menu, select `Controller|Configure` for the following dialog:

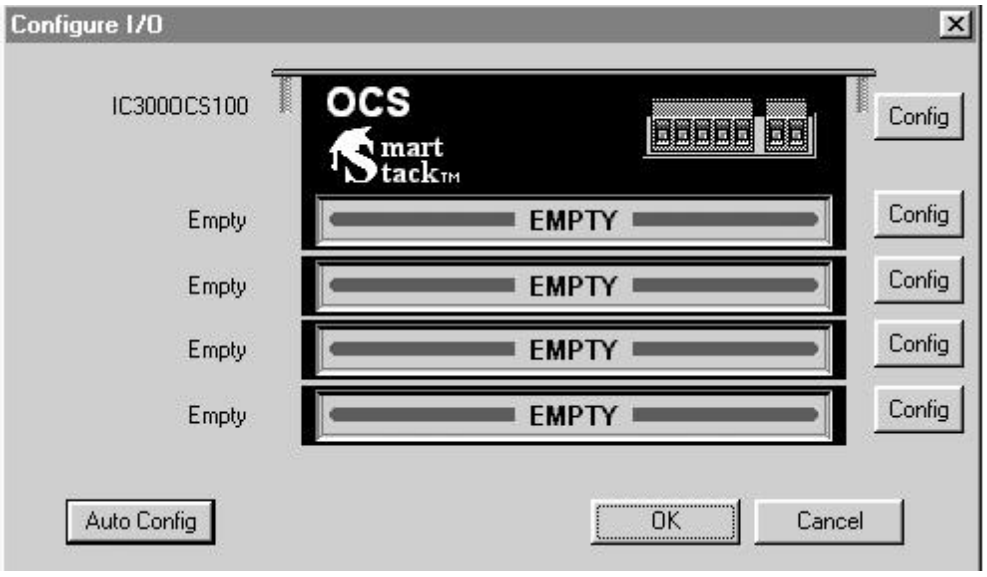


Figure 2.1 – Configure Controller Type Dialog

Note: Ensure that the proper controller is selected. If it is not selected, double-click on the box and select the desired controller from the pull-down menu. Press the OK button [OK].

If the OCS/RCS has one or more SmartStack™ Modules already installed, the user can use AutoConfig to determine and set the I/O automatically. If the controller is not physically attached to Cscape or its SmartStack™ Modules are not available, use the manual configuration.

The user can choose to do the following:

a. Add a SmartStack I/O Module

Caution: For proper functioning and to avoid possible damage, do not install more than four SmartStack™ Modules per controller

1. To place a SmartStack I/O module into an EMPTY 

slot, ADD the module. From the CONFIGURE I/O Dialog, click on the CONFIG button 

to the right of the desired module or double-click on the empty slot.
Either method will invoke the SmartStack Module Selection Dialog:

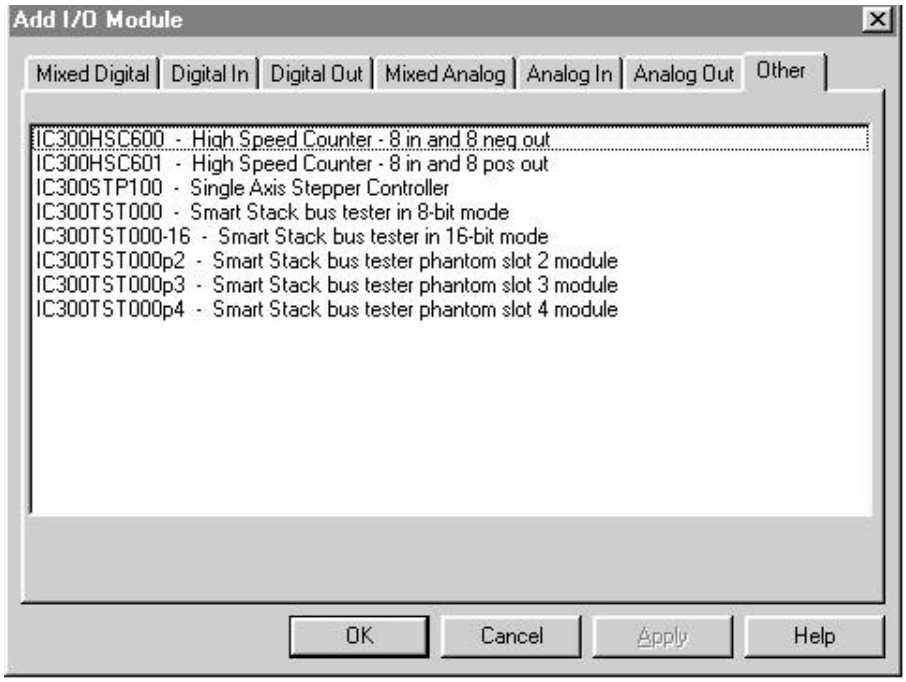


Figure 2.2 – Add I/O Module Screen
("Other" selections are shown.)

2. Use the mouse to select the type of module desired. The HSC600/601 is a specialty module. Select the **Other** Tab. Select the desired module, and click the OK button.

b. Delete a SmartStack Module

If the desired SmartStack slot shows a module already installed, the module can be deleted.

1. Right-click on the picture of the configured slot. A floating menu appears.
2. From the menu, click on `DELETE MODULE`.

c. Select a Different SmartStack Module

If the desired SmartStack slot shows a module already installed, the module can be replaced with a different module.

1. Right-click on the picture of the configured slot. A floating menu appears.
2. From the menu, click on 1. REPLACE MODULE. This invokes the SmartStack Module Selection Dialog.
3. Use the mouse to select the desired module and then click OK [OK] .

2.3 Configuration of HSC600/601 Modules

The screen now depicts the controller and HSC SmartStack Module that has been chosen by the user. The desired module is ready to be configured.

1. Double-click on the picture of the module or click on the Config button [Config] just to the right of the picture.

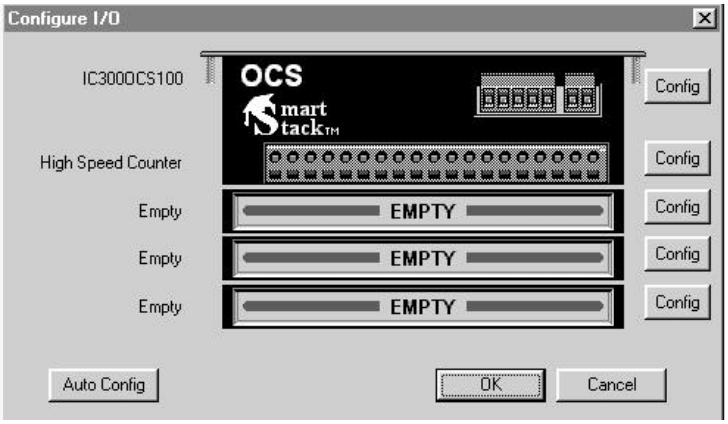


Figure 2.3 – Configure I/O Screen

The Module Configuration Screen appears. Two tabs are available for selection.

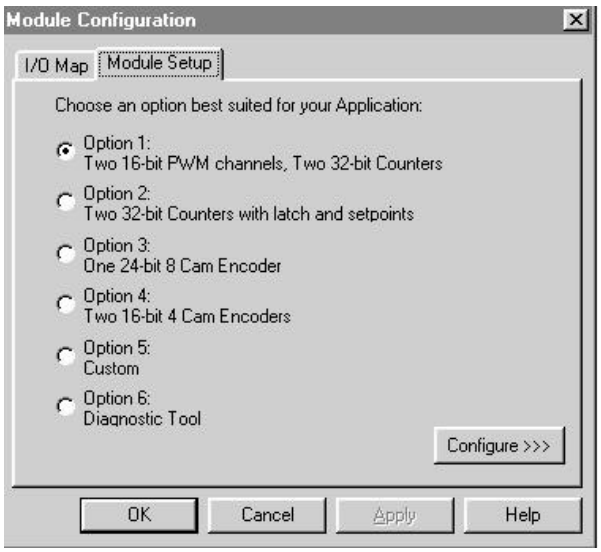


Figure 2.4 – Module Configuration Screen ("Module Setup" Tab Selected)

a. I/O Map Tab (Screen Not Shown)

The I/O Map describes which I/O registers are assigned to a specific SmartStack™ Module. Although there are no user-defined parameters, the I/O Map needs to be viewed after an option is selected and configured to determine where the module is located in the point map. ***Once an option has been configured, the Module Configuration screen reappears, and the user can then select the I/O Map tab to review the settings.***

b. Module Setup Tab

Upon pressing the Module Setup Tab, the Figure 2.4 appears:

1. Select an option.

2. Once an option is selected, check the table of contents for the chapter that covers the option. Each option has its own dedicated chapter that provides operational information and additional configuration procedures for that option.

CHAPTER 3: OPTION 1

Dual 32-Bit Totalizer/Frequency Counter plus Dual 16-Bit PWM/Pulse Outputs

3.1 Option 1 Overview

3.1.1 General

Initial configuration procedures to select Option 1 are contained in Chapter Two. The following topics pertaining to Option 1 are covered in Chapter Three:

a. Functions and capabilities; pin-out
b. Registers
c. I/O Map - shows functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.
d. Configuration procedures
e. Advanced Use-Cscape Override Configuration Procedures – used only for applications needing to override the Cscape setup during runtime. Not used in most applications.

3.1.2 Functions

Option 1 gives the HSC600/601 the capabilities to:

a. Operate as Dual 32-Bit Totalizer Counters with output latches. Each input counter is placed in one of four possible input modes. The input counters can be configured independently.

b. Perform as a Frequency Counter. Both input counters (Channel A and Channel B) on the HSC module are used for this function. Frequency can be measured for Channel A or Channel B or for both channels alternately. The HSC can not operate as a Dual 32-Bit Totalizer Counter when configured for this function.

c. Act as Dual 16-bit PWM/Pulse *Output* Counters. Each Pulse Width Modulator/Pulse Output counter (PWM) can be configured independently. The PWM *Output* Counters are independent of the Totalizer *Input* Counters.

d. Allow Direct I/O Access: Eight inputs and eight outputs are directly accessible in the %I and %Q registers of the Operator Control Station (OCS/RCS).

The functions of Option 1 are covered in greater detail in Sections 3.2 - 3.5.

3.1.3 Safety Warning

Warning: Failure to disable the High Speed Counter Module (HSC600/601) manually through the ladder code program could cause either personal injury or damage to equipment.

When the OCS/RCS is in the Idle or Stop modes, the HSC600/601 continues normal operation. **The user must physically disable the HSC600/601 through the ladder code program.**

3.2 Dual 32-Bit Totalizer Counters Function

3.2.1 Enabling the Totalizers/Counters

The HSC operates as two 32-Bit Totalizer Counters with output latches. Inputs to the HSC are counted/totaled. If this function is desired, one or both of the counters must be enabled during configuration by placing a checkmark in the box next to the applicable counter. One of four possible input modes must be selected for each enabled counter. If both counters are enabled, they can be configured independently of each other. The modes for each counter can differ.

Note: If this function is selected, the HSC can not function as a Frequency Counter.

3.2.2 Inputs to Totalizer Counters

Each counter has the following inputs:

1. Clock / Count Up / Quadrature A
2. Count Direction / Count Down / Quadrature B
3. Count Clear – Clears or resets the count or total.
4. Count Enable - Starts the count/total.
5. Count Load – Forces the count to a preset value
6. Count Latch – Sends out the current counter value in the Read register.

Regardless of the input mode (discussed in the next section), each input counter has four control signals that are used to direct the counter (load, latch, clear and enable). All four control signals are provided to the HSC by the OCS/RCS or two of the signals can be provided as external inputs. Control signals and external inputs are explained in more detail in **Section 3.2.5**.

3.2.3 Counter Input Modes

One of four possible input modes must be selected for each enabled counter.

a. Totalizer Mode

The Totalizer Mode is used in applications that require counting either up or down. An example application is counting items on a production line. The following description explains how the inputs are used for this mode.

The Totalizer counts on each positive **Clock** edge. The **Clock Direction** input causes an up-count (when the input is a logic high) and a down-count (when the input is a logic low).

The **Direction** input of the counter can be configured as an *external input* (no %Q registers*) or register data from the OCS/RCS* (by selecting the **Latch, Load, Clear, and Enable from Ladder** box on the configuration screen). A Load value can be written to the Load Register, and the counter reloads its count to this value when the **Count Load** input is a logic high. The Counter remains at the load value while the **Count Load** input is held at logic high. Counting starts at a logic low. The Counter rolls over at 0 on a down-count and 4,294,967,296 on an up-count. **Count Clear** sets the counter to zero, and **Count Latch** latches a snap-shot of the count value. The **Count Enable** is used to enable/disable counting.

b. Up/Down Mode

The Up/Down Mode is used in applications that require counting up and down. An example application is counting items in a hopper as items are added (count up) and subtracted (count down). The following description explains how the inputs are used in for this mode.

The UP/DOWN counter operates much the same as the Totalizer with the **Clock** and **Direction** inputs conditioned as Clock-Up and Clock-Down inputs. The normal **Clock** input becomes Clock Up and the normal Direction input becomes Clock Down. A Load value can be written to the Load Register, and the counter reload its count to this value when the **Count Load** input is at logic high. The counter remains at the load value while the **Count Load** input is held at logic high. Counting starts at a logic low. The counter rolls over at 0 on a down-count and 4,294,967,296 on an up-count. **Count Clear** sets the counter to zero and **Count Latch** latches a snap-shot of the Count value. The **Count Enable** is used to enable/disable counting.

c. Quadrature Mode

The Quadrature Mode is used in applications where it is necessary to know the position of a motor and the direction/distance it has moved. An example application is the tracking of a rotary encoder. The following description explains how the inputs are used in for this mode.

The Quadrature Counter operates much the same as the Totalizer but it also operates with the **Clock** and **Direction** inputs conditioned as Clock A and Clock B. The normal **Clock** input becomes Clock A and the normal **Direction** input becomes Clock B. The phase relationship of Clock A and Clock B determines the count direction. A Load value can be written to the Load Register and the counter reloads its count to this value when the **Count Load** input is at logic high. The Counter remains at the load value while the **Count Load** input is held at logic high. Counting starts at a logic low. The Counter rolls over at 0 on a down-count and 4,294,967,296 on an up-count. **Count Clear** sets the counter to zero and **Count Latch** latches a snap-shot of the Count value. The **Count Enable** is used to enable/disable counting.

d. Timer Mode

The Timer Mode is used in applications requiring time interval measurements. The following description explains how the inputs are used for this mode.

Each Counter can also be configured to operate with an internal 10MHz clock input. The **Count Direction** can be configured for external input or DIR selected by up/down buttons on the configuration menu.

3.2.4 Input Signal Conditioning

Input modes are affected by how the Clock and Count Direction inputs are conditioned. Conditioning of the input signals is based upon the selections made in the **Input Signal Conditioning** section of the Cscape configuration screen for Option 1. This section allows the user to set the ON/OFF voltages and the frequency for noise filtering. The input voltage threshold and the frequency response is selected from pull-down menus.

3.2.5 Control Signals and External Inputs

a. Control Signals Sent from the Ladder Logic (or from External Sources)

Each input counter has four control signals that are used to direct the counter (load, latch, clear and enable). The control signals are normally provided to the HSC in one of two possible ways via selections made to the Cscape configuration screen.

1. All four control signals are sent to the HSC from the OCS/RCS and are under the control of the ladder program within the OCS/RCS. To use this approach, checkmark the box that is labeled **Latch, Load, Clear, Enable from Ladder** for the applicable counter on the Cscape configuration screen.

   Note: Counter 1 uses registers %Q25-28 for **Latch, Load, Clear, and Enable signals.** Counter 2 uses registers %Q29-32. (See Table 3.9.)

2. Two of the four control signals are received from external sources and are configured as external inputs. *The remaining two control signals are accessible via the control register (%Q) within the OCS/RCS and are under the control of the OCS/RCS ladder program.*

   Note: Although the remaining two control signals fall under the control of the OCS/RCS ladder program, do not checkmark the box labeled **Latch, Load, Clear, Enable from Ladder** when using external inputs.

   The Cscape configuration screen shows that each input counter has two external inputs. Each external input has a pull-down menu that allows the selection of a desired control signal for that input. (Counter One uses External Inputs 3 and 4; Counter Two uses External Inputs 7 and 8.)

b. Types of Control Signals

Each counter (if enabled) is controlled by the following control signals.

CLEAR Setting the Clear signal to Logic 1 clears the counter to zero, and the count remains at zero until the Clear signal is reset to Logic 0

LOAD Setting the Load signal to Logic 1 forces the count to the Load Value. The Count remains at the Load value until the Load signal is reset to Logic 0. The count then starts from that value and increments or decrements depending on the direction of the count.

ENABLE Setting the Enable signal to Logic 1 allows the Counter to count. When the Enable signal is set to Logic 0, counting is inhibited.

LATCH The current counter value is latched into the counter's Read Register on the rising edge of the Latch signal. The counting function is not disturbed by the latch. The register data is not reloaded until the following Latch signal's rising edge appears.

c. External Input and Control Connector

Table 3.1 shows the inputs to the connector (J3) on the HSC. Inputs 1-4 are used for Counter A, and inputs 5-8 are used for Counter B. Each counter has clock and direction inputs as well as external inputs for control signals. Again, if external inputs are selected, *the remaining two control signals are accessible via the control register (%Q) within the OCS/RCS and are under the control of the OCS/RCS ladder program.* Pin 9 of J3 is used for the ground reference.

Table 3.1 – Option 1 Pin-out (J3**)**									
Name	Input1	Input2	Input3	Input4	Input5	Input6	Input7	Input8	
Pin	1	2	3	4	5	6	7	8	9
Usage	CLK A	DIR A	CNTRL A	CNTRL A	CLK B	DIR B	CNTRL B	CNTRL B	GRD

3.2.6 Totalizer Registers

The registers used by the Totalizer Counters in the OCS/RCS are defined by Cscape in Table 3.2.

The Counter Load values are 32 bit values. Each Counter can be loaded with these values, which are typically used in count down operation. %AQ1 DWORD is the Counter A load value. %AQ3 DWORD is the Counter B load value. The Load control is used to load the values into the desired counter. A read of the %AI6 DWORD and %AI8 DWORD register returns the 32 bit counter values latched by the Latch control.

If different parameter levels are desired *during runtime* than those listed on the Option 2 configuration screen, %Q19 (MASK) must be set. (See **Advanced Use –Cscape Override Procedures** in Section 3.8.)

Note: The Cscape Override procedures are <u>not</u> intended for most applications and are recommended only for applications that require parameter changes *during runtime.*

Note: Table 3.2 depicts *all* registers used in Option 1 in addition to the totalizer registers. **It is important to read through this chapter to obtain information covering different kinds of registers.** *For example, information pertaining to Frequency Counter registers (Section 3.3.2) and PWM registers (Section 3.4.4) can be found in the sections specified.* Also, the I/O Map (Table 3.6) contains additional information regarding registers used in Option 1.

Table 3.2 – Totalizer / Frequency Counter Registers *

Register	Description
%I1-8	Inputs 1-8
%I9	Gate Signal for the frequency counter.
%I10-11	Used for PWM A & B.
%I12-16	Not used.
%Q1-8	Outputs 1-8
%Q9-12	Mode A – Normally masked -used during Cscape Override.
%Q13-16	Mode B– Normally masked -used during Cscape Override.
%Q17	Frequency A– Normally masked -used during Cscape Override.
%Q18	Frequency B– Normally masked -used during Cscape Override.
%Q19	Leave set to 0 to preserve Cscape setup. This is the MASK bit.
%Q20-24	Not used.
%Q25-28	Control A
%Q29-32	Control B
%Q33-36	Configuration A– Normally masked -used during Cscape Override.
%Q37-40	Configuration B– Normally masked -used during Cscape Override.
%Q41	Trigger PWM A – Normally masked -used during Cscape Override.
%Q42	Pulse PWM A– Normally masked -used during Cscape Override.
%Q43	X16 PWM A– Normally masked -used during Cscape Override.
%Q44	Out PWM A– Normally masked -used during Cscape Override.
%Q45	Trigger PWM B– Normally masked -used during Cscape Override.
%Q46	Pulse PWM B– Normally masked -used during Cscape Override.
%Q47	Pulse PWM B– Normally masked -used during Cscape Override.
%Q48	Out PWM B– Normally masked -used during Cscape Override.
%Q49-50	V-in– Normally masked -used during Cscape Override.
%Q51-52	Frequency in– Normally masked -used during Cscape Override.
%Q53-56	Not used.
%AI1 WORD	1 (Option number)
%AI2 DWORD	Channel A count or frequency low word
%AI3	Channel A count or frequency high word
%AI4 DWORD	Channel B count or frequency low word
%AI5	Channel B count or frequency high word
%AI6 DWORD	Channel A latch value low word
%AI7	Channel A latch value high word
%AI8 DWORD	Channel B latch value low word
%AI9	Channel B latch value high word
%AQ1 DWORD	Channel A frequency time base low word / Counter A Load Value
%AQ2	Channel A frequency time base high word
%AQ3 DWORD	Channel B frequency time base low word / Counter B Load Value
%AQ4	Channel B frequency time base high word
%AQ5 WORD	Channel A PWM cycle time
%AQ6 WORD	Channel A pulse or PWM on time
%AQ7 WORD	Channel B PWM cycle time
%AQ8 WORD	Channel B pulse or PWM on time
***** Channel A = Counter 1 Channel B = Counter 2	

3.3 Dual Channel Frequency Counter Function

3.3.1 Channel A / Channel B

Option 1 can be configured for a two-channel Frequency Counter function, which uses both counters (Channel A and Channel B). Frequency can be measured at the **A clock input**, the **B clock input** or both the **A and B clock inputs** alternately.

3.3.2 Registers

The registers used by the Frequency Counters in the OCS/RCS are defined by Cscape in Table 3.2.

The time base for the Channel A measurement is loaded into %AQ1 DWORD and the time base for the Channel B measurement is loaded into %AQ3 DWORD. The gate signal is available in %I9. The frequency measurements run automatically at approximately the rate of the time base plus one scan without user intervention. The most recent input A frequency is in %AI2 DWORD, and the most recent input B frequency is in %AI4 DWORD.

Time base Example:

The desired output is in hertz (1 second or 1Hz).
Place 10,000,000 into %AQ1 (or %AQ3) - the time base is in seconds. The frequency output in %AI2 (or %AI4) is in hertz.

3.4 PWM Output Counters

3.4.1 Enabling the PWM Output Counters

Option 1 contains two Pulse Width Modulation (PWM A and PWM B) circuits that are completely independent of the Totalizer Input Counters. PWM outputs are used to vary the length of time that a device or sensor is turned ON or OFF. In PWM, a pulse train consisting of equal-width and equal-amplitude pulses is changed by varying the width of the pulses in accordance with a modulating signal.

If this function is desired, one or both of the counters must be enabled during configuration by placing a checkmark in the box next to the applicable PWM Output Counter. If both counters are enabled, they can be configured independently of each other.

3.4.2 Output Modes

Two independent PWM channels are provided (PWM A and PWM B). Each output counter can be used either in the continuous PWM mode or the One Shot pulse mode. The modes for each counter can differ.

a. The continuous PWM/pulse mode is automatically selected by Cscape unless the user checkmarks the box next to the **One Shot** option. This continuous PWM mode is normally used to control valves, motors, and other devices.

b. The One Shot mode is a single ON pulse triggered by Channel A or Channel B's trigger (%Q41 in the PWM register). The One Shot mode generates a shorter pulse than the ladder program is able to do.

3.4.3 Cycle Time and ON Time

The PWM's are configured by entering a cycle time into the registers for the applicable output counter. The cycle time allows the HSC to define the output frequency, which includes the ON time. Also, an ON time value is entered into the registers (by the user) for the applicable counter, which allows the HSC to determine the duty cycle. (See Table 3.3.)

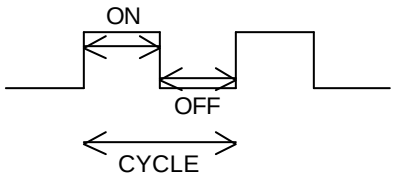


Figure 3.1 – PWM Cycle Time

a. Basic Calculations

Cycle Time = ON time + OFF time.
Duty Cycle = ON time/Cycle Time
Frequency = 1/Cycle Time.

Examples:
An ON time of 0 = 0% duty cycle
An ON time of half the cycle time = 50% duty cycle
An ON time equal to the cycle time = 100% Duty Cycle.

b. Calculating Frequency using Cycle Time

The PWM's are configured by entering a cycle time into registers %AQ5 (for PWM A) and %AQ7 (for PWM B). The PWM cycle time is programmable in 100ns increments from 40µSec to 3,2767mSec. The programmed value represents the number of 100ns counts for an entire cycle. Once the cycle time is entered, the frequency is determined by the HSC. *There are two values that can be entered into the %AQ5 or %AQ7 registers, which have special uses: 1 and 0. See note.*

Example:

A cycle time value of 1000 is entered in Register %AQ5
Cycle Time = 1000 x 100ns = 100 microsecond PWM cycle time
Frequency = 1/Cycle Time = $1/10^{-4}$ = 10KHz.

Note: ***Special use for 1 and 0*****:** A programmed value of 1 causes the internal count to remain at 0 and the PWM output to remain off. A programmed value of 0 sets the cycle time to its maximum value (6.5535ms).

X16 Function: A X16 function is available to multiply the PWM times by 16 and produces a longer cycle time and ON time. This yields a resolution of 1.6us and a maximum cycle time of over 100ms. The x16 function is selected using the configuration screen.

c. Calculating Duty Cycle using ON Time

The PWM ON time is programmable in 100ns increments from zero up to the total cycle time for 100% duty cycle.

Examples:

Duty Cycle = ON time/Cycle Time
A cycle time value of 1000 is entered in Register %AQ5

ON Time entered in Register %AQ6: 0.
Duty Cycle = 0%

ON Time entered in Register %AQ6: 500.
Duty Cycle = 50%

ON Time entered in Register %AQ6: 1000.
Duty Cycle = 100%

X16 Function: The time increments are 1.6us.

3.4.4 PWM Registers

The registers used used by the PWM Output Counters in the OCS/RCS are defined in Table 3.3. . Register numbers below are referenced to the base register numbers for the HSC600 module.

The register blocks shown in white are configured by the user.

The register blocks shown in light gray are normally configured by the Cscape program. If the Cscape configuration is overridden, the user must also configure the blocks in gray. In such cases, refer to Section 3.8, which covers Cscape Override procedures.

Table 3.3– PWM Registers

%I10	PWM A signal.
%I11.	PWM B signal
%Q41	Off to On: Trigger channel A one shot pulse if enabled. On to Off: No effect. Pulse may not be retriggered until it times out.
%Q42	On: Enable channel A one shot mode (stops PWM A). Off: Starts PWM A.
%Q43	On: Multiply channel A cycle and on times by 16. Off: Channels A times are multiples of 100ns.
%Q44	On: Connect channel A signal to HE800HSC600 output 1. Off: Connect %Q1 to output 1.
%Q45	Off to On: Trigger channel B one shot pulse if enabled. On to Off: No effect. Pulse may not be retriggered until it times out.
%Q46	On: Enable channel B one shot mode (s tops PWM B). Off: Starts PWM B.
%Q47	On: Multiply channel B cycle and on times by 16. Off: Channels A times are multiples of 100ns.
%Q48	On: Connect channel B signal to HE800HSC600 output 4. Off: Connect %Q4 to output 4.
%AQ5	Channel A PWM cycle time.
%AQ6	Channel A PWM or pulse on time. Should be no longer than channel A cycle time.
%AQ7	Channel B PWM cycle time.
%AQ8	Channel B PWM or pulse on time. Should be no longer than channel B cycle time.

3.4.5 PWM Connector

Table 3.4 shows the outputs to the connector (J3) on the HSC. Outputs 1-4 are used for PWM A, and outputs 5-8 are used for PWM B. The PWM/pulse signals can be connected to physical outputs under program control. The PWM/pulse signals can also be read back to provide an internal timer or cycle timer function.

Table3.4 – Option 1 Pinout (J3)

Name	Output 1	Output 2	Output 3	Output 4	Output 5	Output 6	Output 7	Output 8		
Pin	10	11	12	13	14	15	16	17	18	19
Use	%Q1 PWM A	%Q2	%Q3	%Q4	%Q5 PWM B	%Q6	%Q7	%Q8	GRD	Power Load

3.4.6 PWM Resolution

The PWM frequency is the inverse of the PWM cycle time. As discussed in Section 3.4.3, the 100ns and 1.6us PWM resolutions produce the following inverse relationships between PWM frequency and effective PWM resolution . Figure 3.2 shows the resolution achieved for a given frequency.

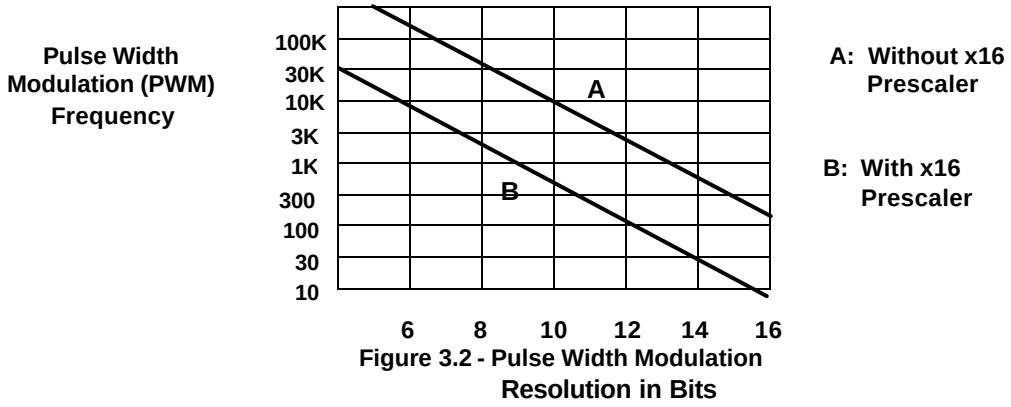


Figure 3.2 - Pulse Width Modulation

3.5 Direct I/O Function

3.5.1 Registers

In the Direct I/O function, the read and write registers are directly accessible as discrete inputs and outputs are turned ON and OFF.

Eight %I and eight %Q registers are used in the Direct I/O function.

Table 3.5 – Direct I/O Registers and Pinout

Register	Signal	Input and Output Pins (J3)
%I1	Input1	1
%I2	Input2	2
%I3	Input3	3
%I4	Input4	4
%I5	Input5	5
%I6	Input6	6
%I7	Input7	7
%I8	Input8	8
%Q1	Output1	10
%Q2	Output2	11
%Q3	Output3	12
%Q4	Output4	13
%Q5	Output5	14
%Q6	Output6	15
%Q7	Output7	16
%Q8	Output8	17

%I and %Q registers are connected to the input and output pins of connector J3. A Read of the %I registers returns the input pins and a write to the %Q registers latches data to the output pins. Two of the output pins (Output 1 and Output 5) can be used as PWM outputs which override the %Q register data. The Read of the %I registers returns data at the input pins regardless of the selected counter mode.

3.6 I/O Map

The I/O Map shows the functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.

The register blocks that are shown in white are normally accessible using the ladder code. The OCS/RCS has a ladder program that the user sets parameters for. If the user does not set parameters for any one of these blocks, the OCS/RCS automatically writes a zero into the block.

The register blocks that are shown in light gray are automatically configured by Cscape if Q19 (the MASK or override bit) is set to 0. This is the normal setup for most applications. However, in dynamic applications that require parameter changes during runtime, the light gray blocks can be overridden. Refer to the final section in Chapter One, which covers Cscape Override procedures. If Cscape Override procedures are used, Q19 is set to 1.

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes during runtime.

The dark gray blocks are not used.

Table 3.6 – I/O Map

%I INPUTS

%I	0	1	2	3	4	5	6	7	8	9
%I 0x		Input1	Input2	Input3	Input4	Input5	Input6	Input7	Input8	GATE
%I 1x	PWMA	PWMB								

%Q OUTPUTS

%Q	0	1	2	3	4	5	6	7	8	9
%Q 0x		Out 1	Out 2	Out 3	Out 4	Out 5	Out 6	Out 7	Out 8	ModeA
%Q 1x	ModeA	ModeA	ModeA	ModeB	ModeB	ModeB	ModeB	FreqA	FreqB	MASK
%Q 2x						CtrlA	CtrlA	CtrlA	CtrlA	CtrlB
%Q 3x	CtrlB	CtrlB	CtrlB	ConfA	ConfA	ConfA	ConfA	ConfB	ConfB	ConfB
%Q 4x	ConfB	TrigA	PulseA	X16A	OutA	TrigB	PulseB	X16B	OutB	V-in
%Q 5x	V-in	Freq-in	Freq-in							

Not used — Configured by Cscape if MASK (%Q19) is not set.

%AI INPUTS

%AI1	WORD	1 (Option number)
%AI2	DWORD	Channel A count or frequency low word
%AI3		Channel A count or frequency high word
%AI4	DWORD	Channel B count or frequency low word
%AI5		Channel B count or frequency high word
%AI6	DWORD	Channel A latch value low word
%AI7		Channel A latch value high word
%AI8	DWORD	Channel B latch value low word
%AI9		Channel B latch value high word

%AQ OUTPUTS

%AQ1	DWORD	Channel A frequency time base low word
%AQ2		Channel A frequency time base high word
%AQ3	DWORD	Channel B frequency time base low word
%AQ4		Channel B frequency time base high word
%AQ5	WORD	Channel A PWM cycle time
%AQ6	WORD	Channel A pulse or PWM on time
%AQ7	WORD	Channel B PWM cycle time
%AQ8	WORD	Channel B pulse or PWM on time

Note: This table serves as a general reference for the starting location of the registers. To determine the *actual* starting location of the various registers, it is necessary to consult the "I/O Map" screen in the Cscape Software *after* configuration. Refer to the following Configuration Procedures in this chapter for more details.

3.7 Option 1 Configuration Procedures

After performing the initial configuration procedures described in Chapter Two, the following procedures are provided to configure Option 1 input and output functions. Also, input signal conditioning parameters must be set including the voltage threshold and the frequency for noise filtering. It is recommended to read the operational information covered this chapter before performing the following steps.

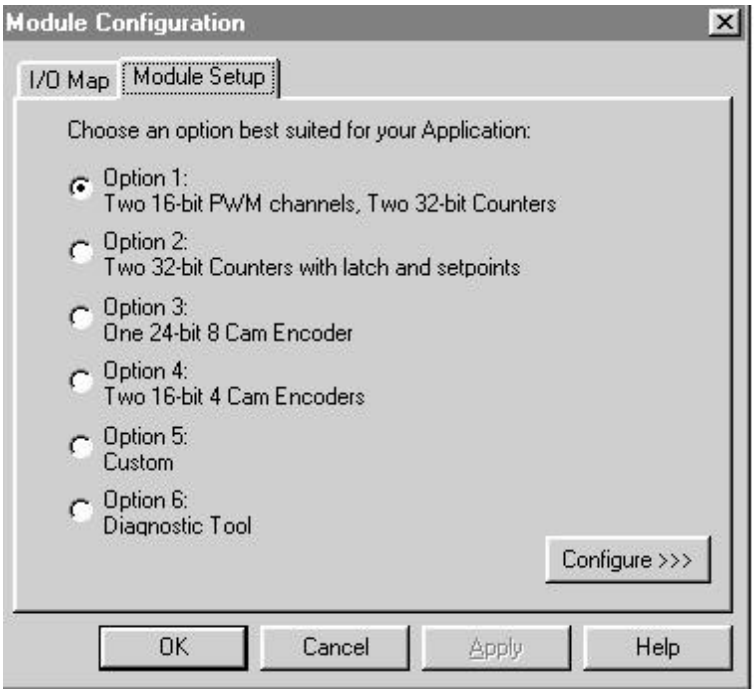


Figure 3.3 – Option 1 Selected

3.7.1 Input Function Configuration

Configure the HSC600/601 for the desired input function(s). If an input function is not desired, the inputs are directly accessible in the OCS/RCS registers. The HSC600/601 can be independently configured as one or two Totalizer Counters or as a Frequency Counter. Follow the procedures specified for the desired input function.

a. If configuring the HSC600/601 as an Input Totalizer Counter:
(Refer to Section 3.3 for register data and other pertinent information covering the the Totalizer Counters.)

Note: For this example configuration, Counter One uses two external control signals; Counter Two uses control signals internally generated from the ladder code)

1. Click the Enable box located next to the desired Totalizer Counter(s). One or both counters can be enabled and can be configured independently. (See Figure 3.3.)

2. Select one of four possible input modes for each enabled counter: (See Section 3.2.3.)
   a. Count/Dir
   b. Up/Down
   c. Quadrature
   d. 10MHz OCS

Note: Counters One and Two do not have to be in the same mode.

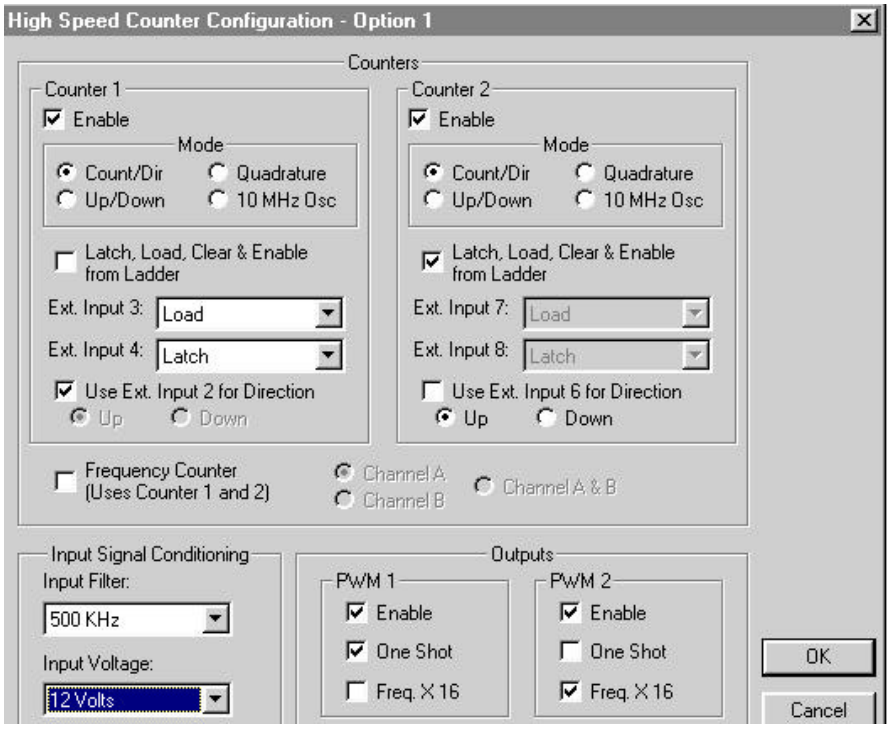


Figure 3.4 – Totalizer Input Counters Selected

3. If the **Count/Dir** mode is selected, it must be determined whether the *Direction Input* is provided via an external input. The choices for the *Direction Input* are located under the mode block for each counter on the Option 1 Screen.

> If an external input is used to determine the *Direction Input* of the count (up or down): Click the box labeled **Use for Ext. Input 2 for Dir**.
>
> If the *Direction Input* is configured by Cscape: Select the appropriate circle labeled **Up** or **Down** to indicate the direction of the count.

Note: The *Direction Input* choices are only visible on the screen if the Count/Dir input mode is selected.

4. Select **control signals** for each enabled Totalizer Counter as discussed in Section 3.2.5. Determine whether all four control signals are wholly generated by the OCS/RCS or if two of the four the control signals are generated from external sources.

The Cscape configuration screen shows that each input counter has two external inputs. Each external input has a pull-down menu that allows the selection of a desired control signal for that input. (Counter One uses controls from External Inputs 3 and 4. Counter Two uses External Inputs 7 and 8.)

Note: External Inputs must not be left floating. They need to be tied to ground or plus as appropriate.

If all four control signals are sent to the HSC600/601 from the OCS/RCS and are under the control of the ladder program within the OCS/RCS: Select the box that is labeled **Latch, Load, Clear, Enable from Ladder** for the applicable counter on the Option 1 Screen.

Note: Counter 1 uses registers %Q25-28 for **Latch, Load, Clear, and Enable signals.** Counter 2 uses registers %Q29-32. (See Table 3.9.)

If two of the four control signals are received from external sources and are configured as external inputs: Select a control signal from the pull-down menus next to **Ext. Input 3** and **External Input 4** for Counter 1 (or **Ext. Input 7** and **Ext. Input 8** for Counter 2). *The remaining two control signals are accessible via the control register (%Q) within the OCS/RCS and are under the control of the OCS/RCS ladder program.*

Note: Although the remaining two control signals fall under the control of the OCS/RCS ladder program, do not click the box labeled **Latch, Load, Clear, Enable from Ladder** when using external inputs.

b. If configuring the HSC600/601 as an Input Frequency Counter:
(Refer to Section 3.4 for register data and other pertinent information covering the Frequency Counter.)

1. To select the **Frequency Counter Mode**, click the box labeled **Frequency Counter –** Uses Counters 1 and 2. Because both input counters (Channel A and Channel B) are required for this function, the HSC can not operate as a Dual 32-Bit Totalizer Counter when configured in the Frequency Counter Mode.

2. Select the channel(s) needing frequency measurement. The frequency can be measured for Channel A or Channel B by clicking the circle next to the desired channel. If frequency measurement is desired for both Channel A and B, click the circle that is labeled **Channel A & B**. In this case, the frequency is measured for both channels alternately. A single counter is used for frequency measurement, and the inputs are multiplexed to provide two channels of measurement. This has the effect of alternately sampling the outputs.(See Figure 3.5.)

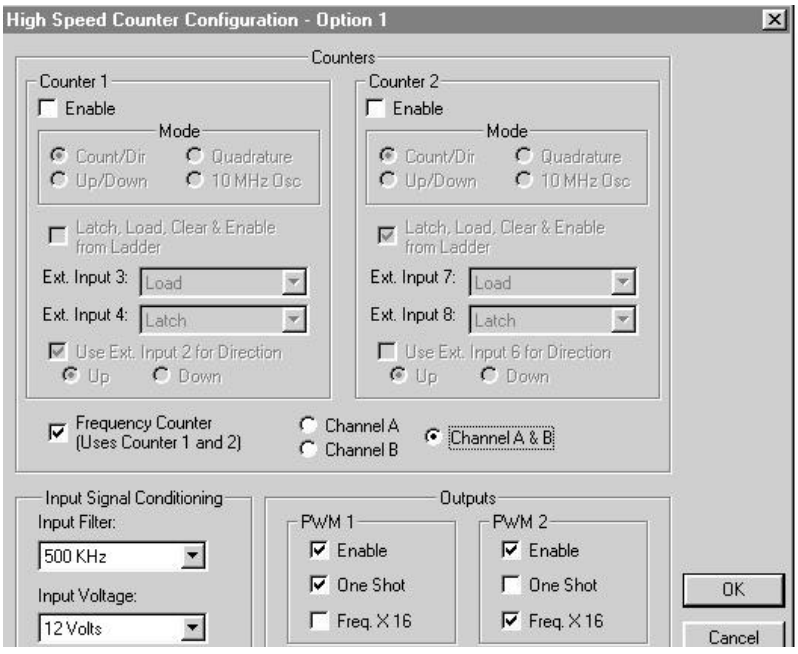


Figure 3.5 – Frequency Input Counter Selected and Pulse Width Modulators (PWM) Enabled

3.7.2 Input Signal Conditioning Configuration

1. The **Input Signal Conditioning** block allows the user to set the input voltage threshold and the input frequency response for noise filtering. It is located on the lower left side of the configuration screen. (See Figure 3.5.)

2. Using the corresponding pull-down menus, select the input voltage and the input frequency for noise filtering. (Refer to Section 3.2.4 for additional information.)

3.7.3 Output Function Configuration

If desired, configure the HSC600/601 for the PWM/pulse output function. (If the PWM/pulse output function is not desired, the outputs are directly accessible in the OCS/RCS registers.) The HSC600/601 can be independently configured as one or two PWM/pulse Output Counters. (See Figure 3.5.)

a. If configuring the HSC600/601 as a PWM/Pulse Output Counter:
(Refer to Section 3.4 for register data and other pertinent information covering the the PWM/pulse Output Counters.)

1. Click the Enable box located under the desired PWM/pulse Counter(s). One or both counters can be enabled and can be configured independently.

2. Select one of two possible output modes for each enabled PWM/pulse Counter: PWM 1 and PWM 2 do not have to be in the same mode. (See Section 3.4.2.)

PWM/pulse Continuous Mode: This mode is not shown on the configuration screen. *Unless the user chooses the One-Shot mode, the Continuous mode is automatically selected.*

One-Shot Mode: To select this mode, click the box labeled **One-Shot**.

3.7.4 Final Configuration Steps and Viewing the I/O Map

After making desired selections, complete the final configuration procedures. It is appropriate to view the I/O Map tab after completing the configuration. The I/O Map shows the number of registers and the starting location of the registers.

1. Press **OK**. The screen reverts to the Module Configuration Screen.

2. Select the **I/O Map** tab. (See Figure 3.6.)

Note: For this configuration example, the I/O Map information shown is not necessarily a true representation of the registers and the starting locations. *It is important to understand how to read the information in the registers for an actual setup*.

Example: If the %I starting location = 10, then what is referred to as %I1 (in this chapter) is really %I10 in the actual I/O Map.

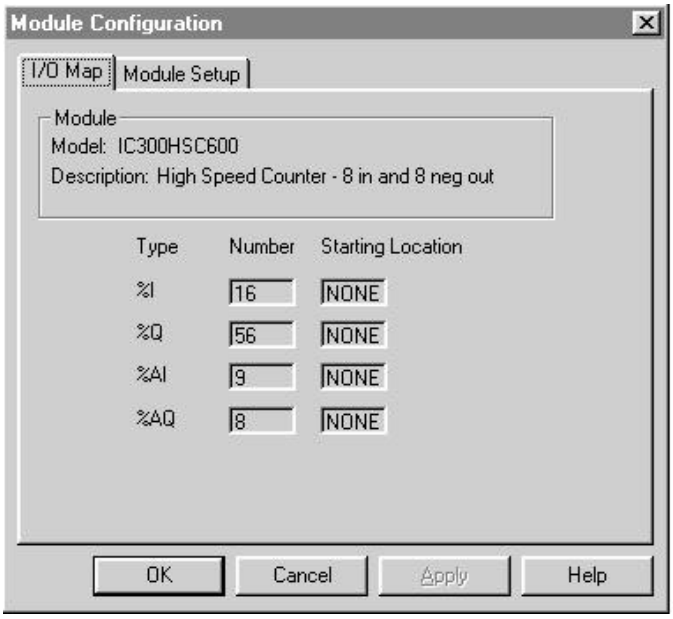


Figure 3.6 – I/O Map Tab

3.8 Advanced Use – Cscape Override Procedures

3.8.1 General

Most application requirements are met using the standard Cscape configuration procedures described earlier in this chapter. The user sets parameters using the Cscape Configuration screen, and the Cscape program has exclusive control over the application at all times. The parameters remain the same (or static) during runtime, and they do not change unless the user reconfigures the setup.

However, there are some applications where it may be necessary to override the Cscape configuration setup during runtime. The HSC600/601 gives the user the flexibility of writing a ladder code program to allow changes to the Cscape parameters during runtime. Such applications are dynamic in that the parameters change when the program is executing. Note that the Cscape configuration is used during power-up and continues until the program overrides the configuration.

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes during runtime.

3.8.2 Overriding Cscape Parameters using a Ladder Code Program

Note: Even if the user intends to change only one register using Cscape Override Procedures, ALL registers must be configured from the ladder code as specified in the Cscape Override section for that option.

A ladder code program must be written to allow the override of the Cscape configuration during runtime. The programmer needs to manually set values into many of the registers that Cscape normally configures.

Although the ladder code program is used during runtime to override the Cscape setup, the standard Cscape configuration procedures must still be performed in order to download the necessary parameters required by the OCS/RCS for power-up. At runtime, the ladder program assumes control and overrides the Cscape configuration parameters.

The following registers need to be manually set using the ladder code program that is written to override the Cscape configuration.

1. Set %Q19 to 1 in the OCS/RCS to override the Cscape configuration of the counter modes, control mapping, frequency counter selection, and other variables.

Table 3.7 – OCS/RCS Register	
Register	**Description**
%Q19	Set to 1.

a. To override the Cscape parameters for the Totalizer Counter Function:

1. Totalizer Input Modes

Configure the counter input modes using the %Q9 through %Q16 registers in the OCS/RCS. %Q9, %Q10, %Q11 and %Q12 select the mode of input. %Q13-16 control count direction. The following table describes the relationship of %Q values and the resulting configuration.

Table 3.8 - %Q Registers and Counter Input Modes				
Counter A Input Mode				
%Q9	%Q10	%Q13	%Q14	Mode
0	0	0	0	Count and Direction
0	1	0	0	Up count / Down count
1	0	0	0	Quadrature
1	1	0	0	Internal 10 MHz clock
0	0	1	0	Always count down
0	0	1	1	Always count up
Counter B Input Mode				
%Q11	%Q12	%Q15	%Q16	Mode
0	0	0	0	Count and Direction
0	1	0	0	Up count / Down count
1	0	0	0	Quadrature
1	1	0	0	Internal 10 MHz clock
0	0	1	0	Always count down
0	0	1	1	Always count up

2. Totalizer Counter Control Signals

The configuration of the counter controls is performed using the %Q25 through %Q40 registers. There are two %Q registers for each of the four input pins that can be used to control the two counters.

%Q33 and %Q34 configure the Input 3 Pin (J3 pin 3) to 1 of the 4 counter control signals of Counter 'A'.
%Q35 and %Q36 configure the Input 4 Pin (J3 pin 4) to 1 of the 4 counter control signals of Counter 'A'.
%Q37 and %Q38 configure the Input 7 Pin (J3 pin 7) to 1 of the 4 counter control signals of Counter 'B'.
%Q39 and %Q40 configure the Input 8 Pin (J3 pin 8) to 1 of the 4 counter control signals of Counter 'B'.

The following table indicates whether the control signals are controlled by the ladder program or by external inputs to the HSC.

The blocks shown in white are normally accessible and can be configured. The blocks shown in light gray are normally configured by Cscape. If overriding the Cscape configuration, the user must set the values for these blocks.

Table 3.9 – Counter A and B Control Override Configuration

Counter A Control							
%Q33	**%Q34**	**%Q35**	**%Q36**	**Load**	**Enable**	**Clear**	**Latch**
0	0	0	0	%Q25	%Q26	%Q27	%Q28
0	0	0	1	%Q25	%Q26	Input4	Input3
0	0	1	0	%Q25	Input4	%Q27	Input3
0	0	1	1	Input4	%Q26	%Q27	Input3
0	1	0	0	%Q25	%Q26	Input3	Input4
0	1	0	1	%Q25	%Q26	0	%Q28
0	1	1	0	%Q25	Input4	Input3	%Q28
0	1	1	1	Input4	%Q26	Input3	%Q28
1	0	0	0	%Q25	Input3	%Q27	Input4
1	0	0	1	%Q25	Input3	Input4	%Q28
1	0	1	0	%Q25	0	%Q27	%Q28
1	0	1	1	Input4	Input3	%Q27	%Q28
1	1	0	0	Input3	%Q26	%Q27	Input4
1	1	0	1	Input3	%Q26	Input4	%Q28
1	1	1	0	Input3	Input4	%Q27	%Q28
1	1	1	**1**	0	%Q26	%Q27	%Q28
Counter B Control							
%Q37	**%Q38**	**%Q39**	**%Q40**	**Load**	**Enable**	**Clear**	**Latch**
0	0	0	0	%Q29	%Q30	%Q31	%Q32
0	0	0	1	%Q29	%Q30	Input8	Input7
0	0	1	0	%Q29	Input8	%Q31	Input7
0	0	1	1	Input8	%Q30	%Q31	Input7
0	1	0	0	%Q29	%Q30	Input7	Input8
0	1	0	1	%Q29	%Q30	0	%Q32
0	1	1	0	%Q29	Input8	Input7	%Q32
0	1	1	1	Input8	%Q30	Input7	%Q32
1	0	0	0	%Q29	Input7	%Q31	Input8
1	0	0	1	%Q29	Input7	Input8	%Q32
0	1	1	0	%Q29	0	%Q31	%Q32
1	0	1	1	Input8	Input7	%Q31	%Q32
1	1	0	0	Input7	%Q30	%Q31	Input8
1	1	0	1	Input7	%Q30	Input8	%Q32
1	1	1	0	Input7	Input8	%Q31	%Q32
1	1	1	1	0	%Q30	%Q31	%Q32

b. To override the Cscape parameters for the Frequency Counter Function:

The following table describes the relationship of %Q values and the resulting configuration.

Table 3.10 – Frequency Counter Control		
%Q17	%Q18	Frequency counter control
0	0	Standard dual totalizer modes
1	0	Measure frequency on A input.
0	1	Measure frequency on B input.
1	1	Measure frequency on A and B inputs alternately.

c. To override the Cscape Input Signal Conditioning:

%Q49 and %Q50 control the input threshold, and %Q51 and %Q52 control the noise filter.

Table 3.11 – Input Signal Conditioning Override		
%Q50	%Q49	Input Threshold
0	0	12 VDC for 24 volt systems.
0	1	6 VDC for 12 volt systems
1	0	1.4 VDC for TTL compatibility
1	1	0 VDC for AC coupled signals
%Q52	%Q51	Noise filter / Maximum Operating Frequency
0	0	High frequency / 1MHz
0	1	Medium frequency / 100KHz
1	X	Low frequency / 10KHz

d. To override the Cscape PWM Output Counters:

The register blocks shown in white are configured by the user.

The register blocks shown in light gray are normally configured by the Cscape program. If Cscape is overridden, the gray blocks must also be configured

Table 3.12 – PWM Registers	
%I10	PWM A signal.
%I11.	PWM B signal
%Q41	Off to On: Trigger channel A one shot pulse if enabled. On to Off: No effect. Pulse may not be retriggered until it times out.
%Q42	On: Enable channel A one shot mode (stops PWM A). Off: Starts PWM A.
%Q43	On: Multiply channel A cycle and on times by 16. Off: Channels A times are multiples of 100ns.
%Q44	On: Connect channel A signal to HE800HSC600 output 1. Off: Connect %Q1 to output 1.
%Q45	Off to On: Trigger channel B one shot pulse if enabled. On to Off: No effect. Pulse may not be retriggered until it times out.
%Q46	On: Enable channel B one shot mode (stops PWM B). Off: Starts PWM B.
%Q47	On: Multiply channel B cycle and on times by 16. Off: Channels A times are multiples of 100ns.
%Q48	On: Connect channel B signal to HE800HSC600 output 4. Off: Connect %Q4 to output 4.
%AQ5	Channel A PWM cycle time.
%AQ6	Channel A PWM or pulse on time. Should be no longer than channel A cycle time.
%AQ7	Channel B PWM cycle time.
%AQ8	Channel B PWM or pulse on time. Should be no longer than channel B cycle time.

NOTES

CHAPTER 4: OPTION TWO

Dual 32 bit Counter with Output Latch, Pre-load Registers, and Two ON/OFF Comparison Outputs per Counter.

4.1 Option 2 Overview

4.1.1 General

Initial configuration procedures to select Option 2 are contained in Chapter Two. The following topics pertaining to Option 2 are covered in Chapter Four:

a. Functions and capabilities; pin-out
b. Registers
c. I/O Map - shows functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.
d. Configuration procedures
e. Advanced Use-Cscape Override Configuration Procedures – used only for applications needing to override the Cscape setup during runtime. Not used in most applications.

4.1.2 Functions

Option 2 gives the HSC600/601 the capabilities to operate as dual 32-Bit Counters with output latches and pre-load registers. The counters (Channel A and Channel B) also have *two* ON/OFFComparison Circuits per counter. When enabled, the ON/OFF Comparison Circuits override ladder control of the output pins. Each counter is placed in one of four possible input modes and can be configured independently. Pre-load values are entered into the appropriate input registers for each counter to indicate the start value of the count.

The outputs of each counter are either sent to the output registers in the Operator Control Station/Remote Control Station (OCS/RCS) *or* are sent to the ON/OFF Comparison Circuits in one or both counters. The ON/OFF Comparison Circuits are used during counting to compare the counter outputs to set-point values, which are determined by the user. Events can be programmed to occur when the ON/OFF set-point values are reached during counting.

The inputs are directly accessible in the %I Registers of the OCS/RCS. Outputs are controllable in the %Q Registers of the OCS/RCS unless the ON/OFF Comparison Circuits are enabled for each counter. Pins 10,11,14, and 15 are controlled by the ON/OFF Comparison Circuits if enabled. Pins 12,13,16, and 17 remain under ladder control.

User information for Option Two is provided starting with Section 4.2.

4.1.3 Safety Warning

Warning: Failure to disable the High Speed Counter Module (HSC600/601) manually through the ladder code program could cause either personal injury or damage to equipment.

When the OCS/RCS is in the Idle or Stop modes, the HSC600/601 continues normal operation. **The user must physically disable the HSC600/601 through the ladder code program.**

4.2 Dual 32-Bit Counters (using Pre-load Register Values) Function

4.2.1 Enabling the Counters

The HSC operates as two 32-Bit Counters with output latches. The user pre-loads the starting count value and determines whether the count is up or down during configuration. If desired, the user also sets ON/OFF set-point values to trigger events to occur (and stop) during the count. If this function is desired, one or both of the counters must be enabled during configuration by placing a checkmark in the box next to the applicable counter. One of four possible input modes must be selected for each enabled counter. If both counters are enabled, they can be configured independently of each other. The modes for each counter can differ.

4.2.2 Inputs to Counters

Each counter has the following inputs:

1. Clock / Count Up / Quadrature A
2. Count Direction / Count Down / Quadrature B
3. Count Clear – Clears or resets the count or total.
4. Count Enable - Starts the count/total.
5. Count Load – Forces the count to a preset value.
6. Count Latch – Sends out the current counter value in the Read register.
7. 10MHz - Internal input

Regardless of the input mode (discussed in the next section), each input counter has four control signals that are used to direct the counter (load, latch, clear and enable). All four control signals are either provided to the HSC by the OCS/RCS via ladder logic (%Q values) or two of the signals can be provided as external inputs. Control signals and external inputs are explained in more detail in Section 4.2.5.

4.2.3 Counter Input Modes

One of four possible input modes must be selected for each enabled counter.

a. Totalizer Mode

The Totalizer Mode is used in applications that require counting either up or down. An example application is counting items on a production line. The following description explains how the inputs are used for this mode.

The Totalizer counts on each positive **Clock** edge. The **Clock Direction** input causes an up count (when the input is a logic high) and a down count (when the input is a logic low).

The **Direction** input of the counter can be configured as an *external input* (no %Q registers*) or register data from the OCS/RCS* (by selecting the **Latch, Load, Clear, and Enable from Ladder** box on the configuration screen). A pre-load value can be written to the Pre-load Register, and the counter reloads its count to this value when the **Count Load** input is a logic high. The Counter remains at the pre-load value while the **Count Load** input is held at logic high. Counting starts at a logic low. The Counter rolls over at 0 on a down count and 4,294,967,296 on an up count. **Count Clear** sets the counter to zero, and **Count Latch** latches a snap-shot of the count value. The **Count Enable** is used to enable/disable counting.

b. Up/Down Mode

The Up/Down Mode is used in applications that require counting up and down. An example application is counting items in a hopper as items are added (count up) and subtracted (count down). The following description explains how the inputs are used for this mode.

The UP/DOWN counter operates much the same as the Totalizer with the **Clock** and **Direction** inputs conditioned as **Clock Up** and **Clock Down** inputs. The normal **Clock** input becomes **Clock Up** and the normal **Direction** input becomes **Clock Down**. A pre-load value can be written to the Load Register, and the counter reload its count to this value when the **Count Load** input is at logic high. The counter remains at the pre-load value while the **Count Load** input is held at logic high. Counting starts at a logic low. The counter rolls over at 0 on a down-count and 4,294,967,296 on an up-count. **Count Clear** sets the counter to zero and **Count Latch** latches a snap-shot of the Count value. The **Count Enable** is used to enable/disable counting.

c. Quadrature Mode

The Quadrature Mode is used in applications where it is necessary to know the position of a motor and the direction/distance it has moved. An example application is the tracking of a rotary encoder. The following description explains how the inputs are used for this mode.

The Quadrature Mode operates much the same as the Totalizer Mode, but it also operates with the **Clock** and **Direction** inputs conditioned as Clock A and Clock B. The normal **Clock** input becomes Clock A, and the normal **Direction** input becomes Clock B. The phase relationship of Clock A and Clock B determines the count direction. A pre-load value can be written to the Pre-load Register, and the counter reloads its count to this value when the **Count Load** input is at logic high. The Counter remains at the pre-load value while the **Count Load** input is held at logic high. Counting starts at a logic low. The Counter rolls over at 0 on a down count and 4,294,967,296 on an up count. **Count Clear** sets the counter to zero and **Count Latch** latches a snap-shot of the Count value. The **Count Enable** is used to enable/disable counting.

d. Timer Mode

The Timer Mode is used in applications requiring time interval measurements. The following description explains how the inputs are used in for this mode.

Each Counter can also be configured to operate with an internal 10MHz clock input. The **Count Direction** can be configured for external input or register data.

4.2.4 Input Signal Conditioning

Input modes are affected by how the Clock and Count Direction inputs are conditioned. Conditioning of the input signals is based upon the selections made in the **Input Signal Conditioning** section of the Cscape configuration screen for Option 2. This section allows the user to set the ON/OFF voltages and the frequency for noise filtering. The input voltage threshold and the frequency response is selected from pull-down menus.

4.2.5 Control Signals and External Inputs

a. Control Signals Sent from the Ladder Logic or from External Sources

Each input counter has four control signals that are used to direct the counter (load, latch, clear and enable). The control signals are normally provided to the HSC in one of two possible ways via selections made to the Cscape configuration screen.

1. All four control signals are sent to the HSC from the OCS/RCS and are under the control of the ladder program within the OCS/RCS. To use this approach, checkmark the box that is labeled **Latch, Load, Clear, Enable from Ladder** for the applicable counter on the Cscape configuration screen.

   Note: Counter 1 uses registers %Q25-28 for **Latch, Load, Clear, and Enable signals.** Counter 2 uses registers %Q29-32. (See Table 4.7.)

2. Two of the four control signals are received from external sources and are configured as external inputs. *The remaining two control signals are accessible via the control register (%Q) within the OCS/RCS and are under the control of the OCS/RCS ladder program.*

   Note: Although the remaining two control signals fall under the control of the OCS/RCS ladder program, do not checkmark the box labeled **Latch, Load, Clear, Enable from Ladder** when using external inputs.

   The Cscape configuration screen shows that each input counter has two external inputs. Each external input has a pull-down menu that allows the selection of a desired control signal for that input. (Channel A uses External Inputs 3 and 4; Channel B uses External Inputs 7 and 8.)

b. Types of Control Signals

Each counter (if enabled) is controlled by the following control signals.

CLEAR Setting the Clear signal to Logic 1 clears the counter to zero, and the count remains at zero until the Clear signal is reset to Logic 0

LOAD Setting the Load signal to Logic 1 forces the count to the Load Value. The Count remains at the Load value until the Load signal is reset to Logic 0. The count then starts from that value and increments or decrements depending on the direction of the count.

ENABLE Setting the Enable signal to Logic 1 allows the Counter to count. When the Enable signal is set to Logic 0, counting is inhibited.

LATCH The current counter value is latched into the counter's Read Register on the rising edge of the Latch signal. The counting function is not disturbed by the latch. The register data is not reloaded until the following Latch signal's rising edge appears.

c. External Input and Control Connector

Table 4.1 shows the inputs to the connector (J3) on the HSC. Inputs 1-4 are used for Channel A, and inputs 5-8 are used for Channel B. Each counter has clock and direction inputs as well as external inputs for control signals. Again, if external inputs are selected, *the remaining two control signals are accessible via the control register (%Q) within the OCS/RCS and are under the control of the OCS/RCS ladder program.*

Table 4.1 – Option 2 Input Pins (J3)									
Name	Input1	Input2	Input3	Input4	Input5	Input6	Input7	Input8	
Pin	1	2	3	4	5	6	7	8	9
Usage	CLK A	DIR A	CNTRL A	CNTRL A	CLK B	DIR B	CNTRL B	CNTRL B	GRD

4.2.6 Pre-load Register Values

Pre-load values are entered into the appropriate input registers for each counter to indicate the start value of the count. The Counter Load values are 32-bit values. Each Counter can be loaded with these values, which are typically used in count down operations. %AQ2 DWORD is the Channel A load value. %AQ4 DWORD is the Channel B load value. The Load control is used to load the values into the desired counter. A read of the %AI2 DWORD and %AI4 DWORD register returns the 32-bit counter values latched by the Latch control.

4.2.7 ON/OFF Comparison Output Circuits

The outputs of each counter are either sent to the output registers in the Operator Control Station/Remote Control Station (OCS/RCS) *or* are sent to each counter's ON/OFF Comparison Circuits. Both Channel A and Channel B have two ON/OFF Comparison Circuits that can be enabled. The ON/OFF Comparison Circuits are used during counting to compare the counter outputs to set-point values, which are determined by the user. Events occur when the ON/OFF set-point values are reached during counting.

For example, a motor can be programmed to turn on when one of Channel A's ON set-point values is reached during counting. The motor can then be programmed to turn off when the OFF set-point value is reached. As stated earlier, each counter has *two* ON/OFF Comparison Circuits that can be enabled and configured independently. Thus, Channel A can be configured to use a *second* ON/OFF Comparison Circuit during the count. A different event can be programmed to occur (and then stop) such as turning a sensor on and off.

The physical inputs are directly accessible using %I registers in the OCS/RCS. The physical outputs are directly controllable using %Q registers in the OCS/RCS unless the comparison circuit associated with a given output is enabled. When enabled, the ON/OFF comparison results override the associated outputs as shown in Table 4.2.

Table 4.2– Option 2 Output Pins (J3)										
Name	Output 1	Output 2	Output 3	Output 4	Output 5	Output 6	Output 7	Output 8		
Pin	10	11	12	13	14	15	16	17	18	19
Use	%Q1 Channel A Set-point 1	%Q2 Channel A Set-point 2	%Q3	%Q4	%Q5 Channel B Set-point 1	%Q6 Channel B Set-point 2	%Q7	%Q8	GRD	Load Power

4.2.8 Counter Registers

The registers used for the counter function in the OCS/RCS are defined by Cscape in Table 4.3. If different parameter levels are desired *during runtime* than those listed on the Option 2 configuration screen, %Q19 (MASK) must be set. (See Advanced Use –Cscape Override Procedures in Section 4.5.)

Note: The Cscape Override procedures are <u>not</u> intended for most applications and are recommended only for applications that require parameter changes *during runtime.*

Note: Table 4.3 depicts *all* registers used in Option 2. **It is important to read through this chapter to obtain information covering different kinds of registers**. Also, the I/O Map (Table 4.5) contains additional information regarding registers used in Option 2.

Table 4.3 – Counter Registers

Register	Description
%I1-8	Inputs 1-8
%Q1-8	Outputs 1-8
%Q9-12	Mode A
%Q13-16	Mode B
%Q17-18	Not used.
%Q19	Leave set to 0 to preserve Cscape setup. This is the MASK bit.
%Q20	C-out– Normally masked -used during Cscape Override.
%Q21	Wrap A– Normally masked -used during Cscape Override.
%Q22	Wrap B– Normally masked -used during Cscape Override.
%Q23-24	Not used.
%Q25-28	Control A.
%Q29-32	Control B
%Q33-36	Configuration A– Normally masked -used during Cscape Override.
%37-40	Configuration B– Normally masked -used during Cscape Override.
%Q41-42	V-in– Normally masked -used during Cscape Override.
%Q43-44	Frequency in– Normally masked -used during Cscape Override.
%AI1 WORD	2 (Option number)
%AI2 DWORD	Counter A value low word
%AI3	Counter A value high word
%AI4 DWORD	Counter B value low word
%AI5	Counter B value high word
%AI6 DWORD	Channel A latch value low word
%AI7	Channel A latch value high word
%AI8 DWORD	Channel B latch value low word
%AI9	Channel B latch value high word
%AQ1 DWORD	Channel A pre-load value low word
%AQ2	Channel A pre-load value high word
%AQ3 DWORD	Channel B pre-load value high word
%AQ4	Channel B pre-load value high word
%AQ5 DWORD	Channel A on set-point 1 low word
%AQ6	Channel A on set-point 1 high word
%AQ7 DWORD	Channel A off set-point 1 low word
%AQ8	Channel A off set-point 1 high word
%AQ9 DWORD	Channel A on set-point 2 low word
%AQ10	Channel A on set-point 2 high word
%AQ11 DWORD	Channel A off set-point 2 low word
%AQ12	Channel A off set-point 2 high word
%AQ13 DWORD	Channel B on set-point 1 low word
%AQ14	Channel B on set-point 1 high word
%AQ15 DWORD	Channel B off set-point 1 low word
%AQ16	Channel B off set-point 1 high word
%AQ17 DWORD	Channel B on set-point 2 low word
%AQ18	Channel B on set-point 2 high word
%AQ19 DWORD	Channel B off set-point 2 low word
%AQ20	Channel B off set-point 2 high word

4.2.9 Direct I/O:

Eight %I registers and eight %Q registers in the OCS/RCS are used by the Direct I/O section.

Table 4.4 – Direct I/O Registers

Register	Signal	PIN
%I1	Input1	1
%I2	Input2	2
%I3	Input3	3
%I4	Input4	4
%I5	Input5	5
%I6	Input6	6
%I7	Input7	7
%I8	Input8	8
%Q1	Output1	10
%Q2	Output2	11
%Q3	Output3	12
%Q4	Output4	13
%Q5	Output5	14
%Q6	Output6	15
%Q7	Output7	16
%Q8	Output8	17

%I and %Q registers are connected to the input and output pins of connector J3. A Read of the %I registers returns the input pins. (The values in the %I registers can be measured at the input pins). A write to the %Q registers latches data to the output pins. (The values in the %Q registers are measured at the output pins.) Four of the output pins, Outputs 1, 2, 5, and 6 can be used as comparison outputs, which override the %Q register data. The Read of the %I registers returns data at the input pins regardless of the selected counter mode.

4.3 I/O Map

The I/O Map shows the functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.

The register blocks that are shown in white are normally accessible using the ladder code. If the user does not set parameters for any one of these blocks, the OCS/RCS automatically writes a zero into the block.

The register blocks that are shown in light gray are automatically configured by Cscape if Q19 (the MASK or override bit) is set to 0. This is the normal setup for most applications. However, in dynamic applications that require parameter changes during runtime, the light gray blocks can be overridden. Refer to the final section in Chapter One, which covers Cscape Override procedures. If Cscape Override procedures are used, Q19 is set to 1.

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes during runtime.

The dark gray blocks are not used.

Table 4.5 – I/O Map

%I	0	1	2	3	4	5	6	7	8	9
%I 0x		Input1	Input2	Input3	Input4	Input5	Input6	Input7	Input8	

%Q	0	1	2	3	4	5	6	7	8	9
%Q 0x		Out 1	Out 2	Out 3	Out 4	Out 5	Out 6	Out 7	Out 8	ModeA
%Q 1x	ModeA	ModeA	ModeA	ModeB	ModeB	ModeB	ModeB			MASK
%Q 2x	C-out	WrapA	WrapB			CtrlA	CtrlA	CtrlA	CtrlA	CtrlB
%Q 3x	CtrlB	CtrlB	CtrlB	ConfA	ConfA	ConfA	ConfA	ConfB	ConfB	ConfB
%Q 4x	ConfB	V-in	V-in	Freq-in	Freq-in					

Not used — Masked if MASK (%Q19) is not set.

%AI1	WORD	2 (Option number)
%AI2	DWORD	Counter A value low word
%AI3		Counter A value high word
%AI4	DWORD	Counter B value low word
%AI5		Counter B value high word
%AI6	DWORD	Channel A latch value low word
%AI7		Channel A latch value high word
%AI8	DWORD	Channel B latch value low word
%AI9		Channel B latch value high word
%AQ1	DWORD	Channel A pre-load value low word
%AQ2		Channel A pre-load value high word
%AQ3	DWORD	Channel B pre-load value high word
%AQ4		Channel B pre-load value high word
%AQ5	DWORD	Channel A on set-point 1 low word
%AQ6		Channel A on set-point 1 high word
%AQ7	DWORD	Channel A off set-point 1 low word
%AQ8		Channel A off set-point 1 high word
%AQ9	DWORD	Channel A on set-point 2 low word
%AQ10		Channel A on set-point 2 high word
%AQ11	DWORD	Channel A off set-point 2 low word
%AQ12		Channel A off set-point 2 high word
%AQ13	DWORD	Channel B on set-point 1 low word
%AQ14		Channel B on set-point 1 high word
%AQ15	DWORD	Channel B off set-point 1 low word
%AQ16		Channel B off set-point 1 high word
%AQ17	DWORD	Channel B on set-point 2 low word
%AQ18		Channel B on set-point 2 high word
%AQ19	DWORD	Channel B off set-point 2 low word
%AQ20		Channel B off set-point 2 high word

Note: This table serves as a general reference for the starting location of the registers. To determine the *actual* starting location of the various registers, it is necessary to consult the "I/O Map" screen in the Cscape Software *after* configuration. Refer to the following Configuration Procedures in this chapter for more details.

4.4 Option 2 Configuration Procedures

After performing the initial configuration procedures described in Chapter Two, the following procedures are provided to configure Option 2 input and output functions. Also, input signal conditioning parameters must be set including the voltage threshold and the frequency for noise filtering. It is recommended to read the operational information covered this chapter before performing the following steps.

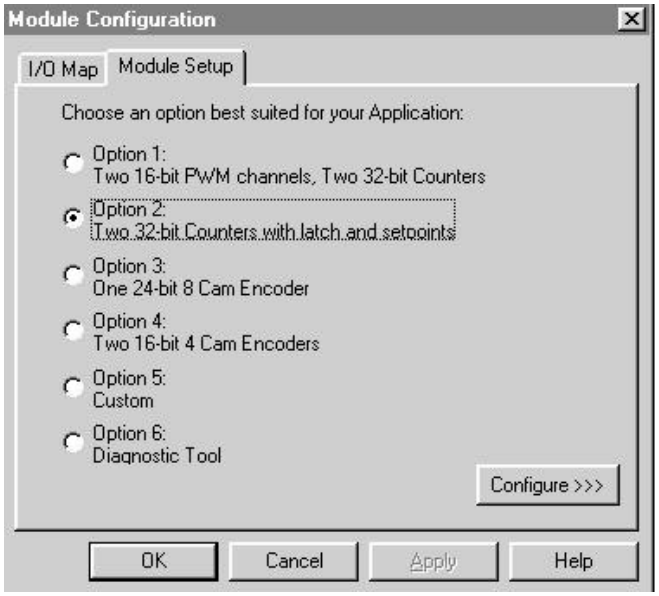


Figure 4.1 – Option 2 Selected

4.4.1 32-Bit Counter Function Configuration

Configure the HSC600/601 for the counter function. The inputs are directly accessible in the OCS/RCS registers. The HSC600/601 can be independently configured as one or two 32-Bit Counters. (Refer to Section 4.2 for register data and other pertinent information covering the 32-Bit Counters.)

1. Click the Enable box located next to the desired counter(s). One or both counters (Channel A or Channel B) can be enabled and configured independently. (See Figure 4.2.)

2. Select one of four possible input modes for each enabled counter:
   a. Count/Dir
   b. Up/Down
   c. Quadrature
   d. 10MHz OCS.

Note: Channel A and Channel B do not have to be in the same mode.

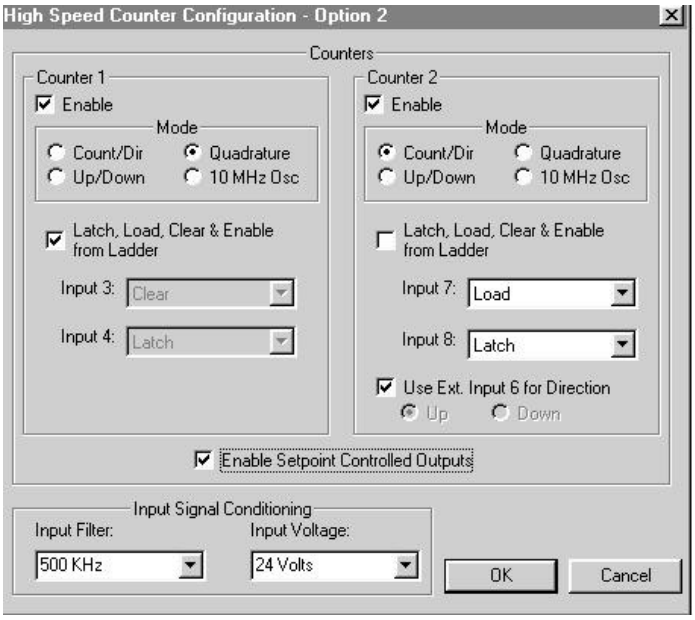


Figure 4.2 – 32-Bit Counters Selected

3. If the **Count/Dir** mode is selected, it must be determined whether the *Direction Input* is provided via an external input or via the OCS/RCS registers. The choices for the *Direction Input* are located under the mode block for each counter on the Option 2 Screen.

   If an external input is used to determine the *Direction Input* of the count (up or down): Click the box labeled **Use for Ext. Input 2 for Dir**.

   If the *Direction Input* is configured using Cscape: Select the appropriate circle labeled **Up** or **Down** to indicate the direction of the count.

Note: The *Direction Input* choices are only visible on the screen if the Count/Dir input mode is selected.

4. Select **control signals** for each enabled 32-Bit Counter. Determine whether all four control signals are wholly generated by the OCS/RCS or if two of the four the control signals are generated from external sources.

The Cscape configuration screen shows that each input counter has two external inputs. Each external input has a pull-down menu that allows the selection of a desired control signal for that input. (Channel A uses controls from External Inputs 3 and 4. Channel B uses External Inputs 7 and 8.)

If all four control signals are sent to the HSC600/601 from the OCS/RCS and are under the control of the ladder program within the OCS/RCS: Select the box that is labeled **Latch, Load, Clear, Enable from Ladder** for the applicable counter on the Option 2 Screen.

Note: Counter 1 uses registers %Q25-28 for **Latch, Load, Clear, and Enable signals.** Counter 2 uses registers %Q29-32. (See Table 4.7.)

If two of the four control signals are received from external sources and are configured as external inputs: Select a control signal from the pull-down menus next to **Ext. Input 3** and **External Input 4** for Counter 1 (or **Ext. Input 7** and **Ext. Input 8** for Counter 2). *The remaining two control signals are accessible via the control register (%Q) within the OCS/RCS and are under the control of the OCS/RCS ladder program.*

Note: Although the remaining two control signals fall under the control of the OCS/RCS ladder program, do not click the box labeled **Latch, Load, Clear, Enable from Ladder** when using external inputs.

4.4.2 Input Signal Conditioning Configuration

1. The **Input Signal Conditioning** block allows the user to set the input voltage threshold and the input frequency response for noise filtering. It is located on the lower left side of the configuration screen. (See Figure 4.2.)

2. Using the corresponding pull-down menus, select the input voltage and the input frequency for noise filtering.

4.4.3 Output Function Configuration

Refer to Section 4.2.8 for register data and other pertinent information covering the ON/OFF Comparison Circuits output function.

1. If the ON/OFF Comparison Circuit output function is desired, click the box labeled **Enable Set-point Controlled Outputs**. (See Figure 4.2.)

2. If the function is not desired, the outputs are directly accessible in the OCS/RCS registers.

4.4.4 Final Configuration Steps and Viewing the I/O Map

After making desired selections, complete the final configuration procedures. It is appropriate to view the I/O Map tab after completing the configuration.

1. Press **OK**. The screen reverts back to the Module Configuration Screen.

2. Select the **I/O Map** tab. The I/O Map shows the number of registers and the starting location of the registers. (See Figure 4.3.)

Note: For this configuration example, the I/O Map information shown is not necessarily a true representation of the registers and the starting locations. *It is important to understand how to read the information in the registers for an actual setup*.

Example: If the %I starting location = 10, then what is referred to as %I1 (in this chapter) is really %I10 in the actual I/O Map.

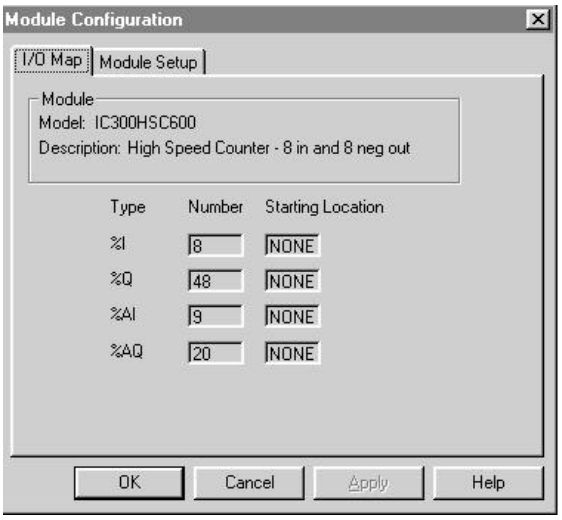


Figure 4.3 –I/O Map Tab

4.5 Advanced Use – Cscape Override Procedures

4.5.1 General

Most application requirements are met using the standard Cscape configuration procedures described earlier in this chapter. The user sets parameters using the Cscape Configuration screen, and the Cscape program has exclusive control over the application at all times. The parameters remain the same (or static) during runtime, and they do not change unless the user reconfigures the setup.

However, there are some applications where it may be necessary to override the Cscape configuration setup during runtime. The HSC600/601 gives the user the flexibility of writing a ladder code program to allow changes to the Cscape parameters during runtime. Such applications are dynamic in that the parameters change when the program is executing. Note that the Cscape configuration is used during power-up and continues until the program overrides the configuration.

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes during runtime.

4.5.2 Overriding Cscape Parameters using a Ladder Code Program

Note: Even if the user intends to change only one register using Cscape Override Procedures, ALL registers must be configured from the ladder code as specified in the Cscape Override section for that option.

A ladder code program must be written to allow the override of the Cscape configuration during runtime. The programmer needs to manually set values into many of the registers that Cscape normally configures.

Although the ladder code program is used during runtime to override the Cscape setup, the standard Cscape configuration procedures must still be performed in order to download the necessary parameters required by the OCS/RCS for power-up. At runtime, the ladder program assumes control and overrides the Cscape configuration parameters.

The following registers need to be manually set using the ladder code program that is written to override the Cscape configuration.

1. Set %Q19 to 1 in the OCS/RCS to override the Cscape configuration of the counter modes, control mapping, and other variables.

Table 4.6 – OCS/RCS Registers	
Register	**Description**
%Q19	Set to 1.

a. To override the Cscape parameters for the 32-Bit Counter Function:

1. Counter Input Modes

Configure the counter input modes using the %Q9 through %Q16 registers in the OCS/RCS. %Q9, %Q10, %Q11 and %Q12 select the mode of input. %Q13 –Q16 control count direction. The following table describes the relationship of %Q values and the resulting configuration.

Table 4.7 - %Q Registers and Counter Input Modes				
Counter A Input Mode				
%Q9	%Q10	%Q13	%Q14	Mode
0	0	0	0	Count and Direction
0	1	0	0	Up count / Down count
1	0	0	0	Quadrature
1	1	0	0	Internal 10 MHz clock
0	0	1	0	Always count down
0	0	1	1	Always count up
Counter B Input Mode				
%Q11	%Q12	%Q15	%Q16	Mode
0	0	0	0	Count and Direction
0	1	0	0	Up count / Down count
1	0	0	0	Quadrature
1	1	0	0	Internal 10 MHz clock
0	0	1	0	Always count down
0	0	1	1	Always count up

2. 32-Bit Counter Control Signals

The configuration of the counter controls is performed using the %Q25 through %Q40 registers. There are two %Q registers for each of the four input pins that can be used to control the two counters.

%Q33 and %Q34 configure the Input 3 Pin (J3 pin 3) to 1 of the 4 counter control signals of Channel 'A'.
%Q35 and %Q36 configure the Input 4 Pin (J3 pin 4) to 1 of the 4 counter control signals of Channel 'A'.
%Q37 and %Q38 configure the Input 7 Pin (J3 pin 7) to 1 of the 4 counter control signals of Channel 'B'.
%Q39 and %Q40 configure the Input 8 Pin (J3 pin 8) to 1 of the 4 counter control signals of Channel 'B'.

The following table indicates whether the control signals are controlled by the ladder program or by external inputs to the HSC. The blocks shown in white are normally accessible and can be configured. The blocks shown in light gray are normally configured by Cscape. If overriding the Cscape configuration, the user must set the values for these blocks.

Table 4.8 – Counter A and B Control Override Configuration

Counter A Control							
%Q33	**%Q34**	**%Q35**	**%Q36**	**Load**	**Enable**	**Clear**	**Latch**
0	0	0	0	%Q25	%Q26	%Q27	%Q28
0	0	0	1	%Q25	%Q26	Input4	Input3
0	0	1	0	%Q25	Input4	%Q27	Input3
0	0	1	1	Input4	%Q26	%Q27	Input3
0	1	0	0	%Q25	%Q26	Input3	Input4
0	1	0	1	%Q25	%Q26	0	%Q28
0	1	1	0	%Q25	Input4	Input3	%Q28
0	1	1	1	Input4	%Q26	Input3	%Q28
1	0	0	0	%Q25	Input3	%Q27	Input4
1	0	0	1	%Q25	Input3	Input4	%Q28
1	0	1	0	%Q25	0	%Q27	%Q28
1	0	1	1	Input4	Input3	%Q27	%Q28
1	1	0	0	Input3	%Q26	%Q27	Input4
1	1	0	1	Input3	%Q26	Input4	%Q28
1	1	1	0	Input3	Input4	%Q27	%Q28
1	1	1	**1**	0	%Q26	%Q27	%Q28
Counter B Control							
%Q37	**%Q38**	**%Q39**	**%Q40**	**Load**	**Enable**	**Clear**	**Latch**
0	0	0	0	%Q29	%Q30	%Q31	%Q32
0	0	0	1	%Q29	%Q30	Input8	Input7
0	0	1	0	%Q29	Input8	%Q31	Input7
0	0	1	1	Input8	%Q30	%Q31	Input7
0	1	0	0	%Q29	%Q30	Input7	Input8
0	1	0	1	%Q29	%Q30	0	%Q32
0	1	1	0	%Q29	Input8	Input7	%Q32
0	1	1	1	Input8	%Q30	Input7	%Q32
1	0	0	0	%Q29	Input7	%Q31	Input8
1	0	0	1	%Q29	Input7	Input8	%Q32
0	1	1	0	%Q29	0	%Q31	%Q32
1	0	1	1	Input8	Input7	%Q31	%Q32
1	1	0	0	Input7	%Q30	%Q31	Input8
1	1	0	1	Input7	%Q30	Input8	%Q32
1	1	1	0	Input7	Input8	%Q31	%Q32
1	1	1	1	0	%Q30	%Q31	%Q32

Table 4.9 – Additional Control Registers	
%Q20	Mode
0	All outputs driven by %Q registers.
1	Comparison results on Outputs 1,2,5, and 6.

b. To override the Cscape Input Signal Conditioning:

%Q41 and %Q42 control the input threshold, and %Q43 and %Q44 control the noise filter.

Table 4.10 – Input Signal Conditioning Override		
%Q42	%Q41	Input Threshold
0	0	12 VDC for 24 volt systems.
0	1	6 VDC for 12 volt systems
1	0	1.4 VDC for TTL compatibility
1	1	0 VDC for AC coupled signals
%Q44	%Q43	Noise filter / Maximum Operating Frequency
0	0	High frequency / 1MHz
0	1	Medium frequency / 100KHz
1	X	Low frequency / 10KHz

NOTES

CHAPTER 5: OPTION 3

24-Bit Electronic Cam with Eight Combinable ON and OFF Functions.

5.1 Option 3 Overview

5.1.1 General

Initial configuration procedures to select Option 3 are contained in Chapter Two. The following topics pertaining to Option 3 are covered in Chapter Five:

a. Functions and capabilities; pin-out
b. Registers
c. I/O Map - shows functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.
d. Configuration procedures
e. Advanced Use-Cscape Override Configuration Procedures – used only for applications needing to override the Cscape setup during runtime. Not used in most applications.

5.1.2 Functions

Option 3 gives the HSC600/601 the capabilities to:

a. Operate as a 24-Bit Electronic Cam with eight combinable ON and OFF functions and to support high resolution encoders.

b. Allow Direct I/O Access: Eight %I and seven %Q registers are directly accessible in the %I and %Q registers of the Operator Control Station (OCS/RCS).

5.1.3 Safety Warning

Warning: Failure to disable the High Speed Counter Module (HSC600/601) manually through the ladder code program could cause either personal injury or damage to equipment.

When the OCS/RCS is in the Idle or Stop modes, the HSC600/601 continues normal operation. **The user must physically disable the HSC600/601 through the ladder code program.**

5.2 Electronic Cam Function

5.2.1 Cam Operation

The electronic cam consists of a 24-bit counter that can be programmed for any number of total counts per revolution up to 16,777,216. In Option 3, the electronic cam is able to control up to eight ON/OFF events. The following explanation provides a general overview of cam operation using an encoder. (See Figure 5.1.)

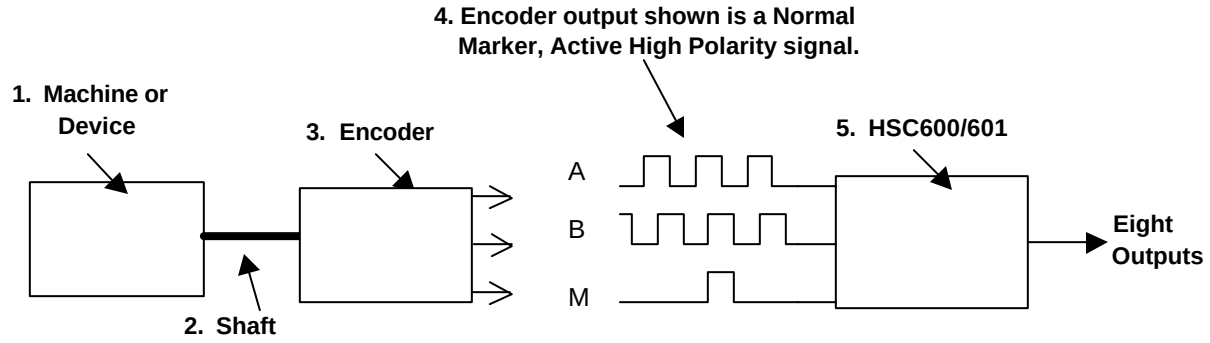


Figure 5.1 – General Overview of Cam Operation using an Encoder (Drawing Not to Scale)

1. A **machine** or other device causes a shaft to rotate.

2. The **shaft** is connected to an encoder. An encoder is a device used to determine the position of a motor as well as the direction and distance that the motor has moved.

3. The **encoder** sends outputs to the HSC600/601 that are in a specific format depending upon the encoder used. (The user needs to consult the encoder manufacturer's manual to determine the encoder's output format.) In order to properly configure the HSC600/601, it is necessary to know the type of signals that the encoder is sending to it.

4. Typical **encoder output signals** are depicted in **Figures 5.1 – 5.8**. The HSC600/601 cam counter is normally driven by a **A quad B** quadrature signal from a rotary encoder. Quadrature outputs consist of A and B signals as well as a marker signal. Signal A needs to be 90° in or out-of phase with the Signal B. The marker signal represents zero as the encoder completes a revolution. The marker signal must always be in sync with the B signal, but the polarities can differ.

The encoder output signal shown in **Figure 5.1 (and Figure 5.2)** is a Normal Marker with active high polarity. This means that the marker is synced with Signal B and has a positive polarity when Signal B is high. The user must know the characteristics of the encoder output signal in order to properly configure the HSC600/601.

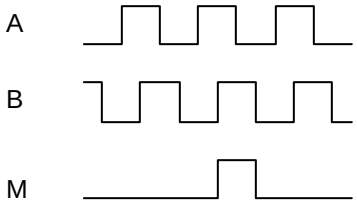


Figure 5.2 – Normal Marker, Active High Polarity

Interpretation of Other Encoder Ouput Signals:

With A quad B signals, the counter increments on each edge, i.e. 4X mode. In **Figure 5.3,** the interpretation of the A and B phase is such that a rising edge on A with B low is an UP count. (Signal A leads B by 90°.) In **Figure 5.4**, the interpretation of the A and B phase is such that a falling edge on A with B low is a DOWN count. (Signal B leads Signal A by 90°.) This describes just one of the four counts per encoder A-B cycle.

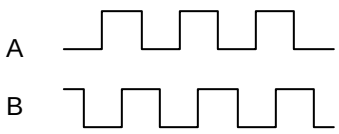


Figure 5.3 - Count UP (4x)

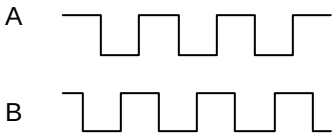


Figure 5.4 - Count DOWN (4x)

In **Figure 5.5**, the marker is active high and 180° out-of-phase with Signal B. In **Figure 5.6**, the marker is inverted active low and is in phase with Signal B. In **Figure 5.7**, the marker is active low and 180° out-of-phase with Signal B.

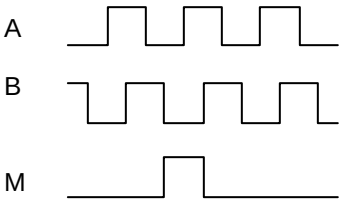


Figure 5.5 – Reverse Phase Marker, Active High Polarity

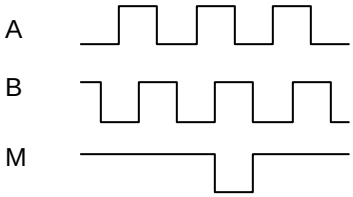


Figure 5.6 – Normal Marker, Active Low Polarity

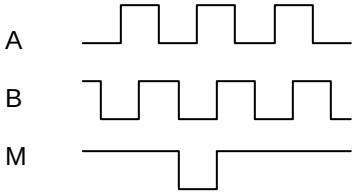
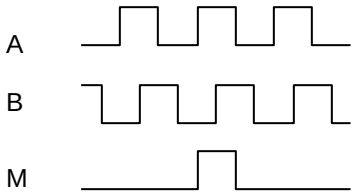


Figure 5.7 – Reverse Phase Marker, Active Low Polarity

In **Figure 5.8**, the marker logic expects the marker to be synchronized with the B input so that there is only one A edge during the marker active interval. If the marker is synchronized with the nominal A channel on the encoder, exchange the A and B channels at the connector.



Note: Swap A and B channels at connector and rename them so that the marker is synchronized with the new B channel.

Figure 5.8 – Marker Synchronized with Channel A

5. In Option 3, the **HSC600/601** acts as an electronic cam, which is able to control up to eight ON/OFF events. ON/OFF events are caused electronically. Examples of ON/OFF events include turning a motor or a switch on and off. The following aspects of cam operation are necessary to understand in order to properly configure the HSC600/601.

Set-points

There are eight cam lobe switches within the HSC600/601, and each switch has a separately programmed ON count and OFF count. The ON and OFF counts are referred to as set-point values. There are high and low set-point values, which are determined by the user. Events can be programmed to occur when the ON/OFF set-point values are reached during counting. For more information on set-points and %AQ registers, refer to Section 5.2.2 and Section 5.4 (Table 5.4.)

Merging Outputs – Combining Events

The outputs can be merged in various combinations for multiple on/off cycles per revolution for a given output. The merge is configured using the Cscape Software or by using the Cscape Override Configuration Procedures located in Section 5.6.

Each switch is normally connected to a separate output pin so that there is one ON/OFF event for each of the output channels. (In Option 3, there are eight output channels.) However, it also possible to configure the HSC600/601 so that the outputs are merged in various combinations for multiple pulse per revolution functions. A *maximum* of eight ON/OFF events can be merged in the HSC600/601 using Option 3. If eight events are merged, the output channel must be Channel 8.

Note: When merging events, the output channel is the highest channel number.

Proper Configuration of Input Signals from the Encoder

When configuring the HSC600/601 in Option 3, the marker polarity and phase can be programmed to match a particular encoder format. The counter total count is normally set to the same number of counts as the encoder resolution but can be set to a higher number for multi-revolution applications such as for a linear cam. In this case the encoder marker should be masked for all revolutions (using marker disable) except for the home section by keeping the marker disable input high while out of the home section. The marker disable input should be tied low for normal operation. Marker and marker disable inputs are provided in the HSC600/601.

The marker phase may be specified to support encoders with the marker channel synchronized to the low phase or the high phase of the B input. The marker polarity may be specified to support encoders with active high or active low marker outputs.

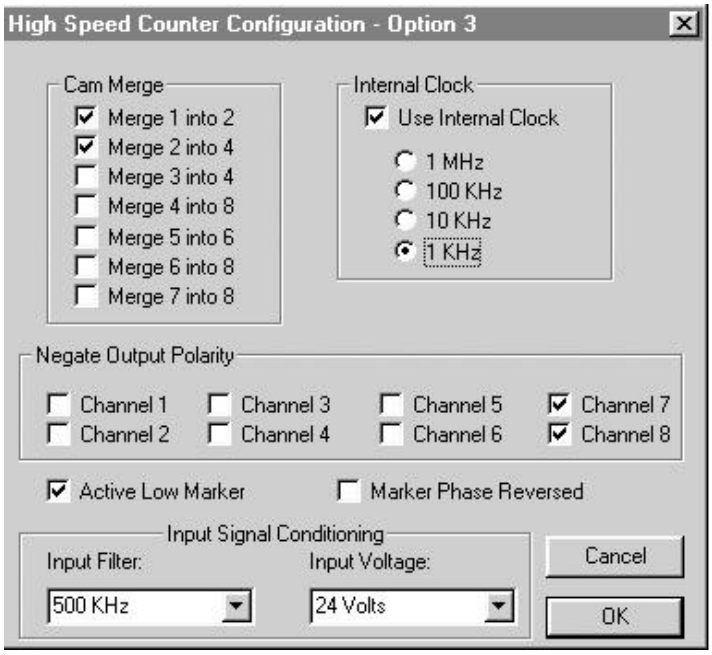


Figure 5.9 – Option 3 Configuration Screen

Internal Clock (Used for Time-Based Applications)

If an encoder is not used, the counter can be clocked by an internal selectable, programmable clock signal to create a flexible electronic pulse / timing generator with up to 1µs resolution with a programmable repeat time of up to four hours. An asynchronous reset is provided using the %Q20 register. Write a zero to this register for normal operation. See Section 5.2.5 (Table 5.2).

Advanced Use – Cscape Override Procedures

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes *during runtime*.

The marker configuration, counter clock source, and output merges are configured by Cscape. If the mask bit, %Q8, is set to 1, the Cscape configuration is overridden by Registers %Q9 through %Q28. (See the Cscape Override Configuration Procedures located in **Section 5.6.**) Each of the cam ON and OFF times and the number of counts per revolution are set using DWORD %AQ registers.

5.2.2 Set-points

There are eight cam lobe switches within the HSC600/601, and each switch has a separately programmed ON count and OFF count. The ON and OFF counts are referred to as set-point values. There are high and low set-point values, which are determined by the user. Events can be programmed to occur when the ON/OFF set-point values are reached during counting

Normally, the ON time uses the low set-point, and the OFF time uses the high set-point. However if required, the user can configure the HSC600/601 to invert the set-point values by marking the **Negate Output Polarity** block on the Option 3 configuration screen.

Each set-point pair defines a count range and is bracketed by the low and high set-points, in which the cam signal is active. For proper operation, the high set-point is always numerically higher than the low set-point. If the maximum count is less than the high set-point, the maximum count becomes the high set-point. If the maximum count is less than the low set-point, the cam signal never becomes active. The output polarity selection in Cscape defines whether the active range is on / positive polarity or off / negative polarity. See Section 5.4 (Table 5.4) for information on %AQ Registers.

The example below uses a low set-point of 200 and a high set-point of 400.

COUNT	POLARITY	OUTPUT
100	POSITIVE	OFF
300	POSITIVE	ON
500	POSITIVE	OFF
100	NEGATIVE	ON
300	NEGATIVE	OFF
500	NEGATIVE	ON

5.2.3 Connector

Table 5.1 lists the A and B signals, M, M disable inputs, and cam signal outputs.

Table 5.1 – Option 3 Pin-out (J3)

Name	Input1	Input2	Input3	Input4	Input5	Input6	Input7	Input8
Pin	1	2	3	4	5	6	7	8
Use	A	B	M	M disable	General purpose	General purpose	General purpose	General purpose
Pin	10	11	12	13	14	15	16	17
Use	CAM 1/ Output 1	CAM 2/ Output 2	CAM 3/ Output 3	CAM 4/ Output 4	CAM 5/ Output 5	CAM 6/ Output 6	CAM 7/ Output 7	CAM 8
Pin	9	18	19					
Use	Input Common	Output Common	Output Power					

5.2.4 Cam Registers

The registers used by the electronic cam function are defined in Table 5.2.

If different parameter levels are desired *during runtime* than those listed on the Option 3 configuration screen, %Q8 (MASK) must be set. (See **Advanced Use –Cscape Override Procedures** in Section 5.6.)

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes *during runtime.*

Note: Table 5.2 depicts *all* registers used in Option 3. **It is important to read through this chapter to obtain information covering different kinds of registers**. Also, the I/O Map (Table 5.4) contains additional information regarding registers used in Option 3.

Table 5.2 – Cam Registers

Registers	Signal
%I1-8	Inputs 1-8
%I9-16	Reads output states of %I inputs 1-8
%Q1-7	Outputs 1-7
%Q8	Leave set to 0 to preserve the Cscape configuration setup. This is the MASK (override) bit.
%Q9	Output 1 merge 1- Normally masked – used only during Cscape Override.
%Q10	Output 2 merge 2- Normally masked – used only during Cscape Override.
%Q11	Output 3 merge 3- Normally masked – used only during Cscape Override.
%Q12	Output 4 merge 4- Normally masked – used only during Cscape Override.
%Q13	Output 5 merge 5- Normally masked – used only during Cscape Override.
%Q14	Output 6 merge 6- Normally masked – used only during Cscape Override.
%Q15	Output 7 merge - Normally masked – used only during Cscape Override.
%Q16	Not used – for internal use.
%Q17	Marker Polarity- Normally masked – used only during Cscape Override.
%Q18	Marker Phase- Normally masked – used only during Cscape Override.
%Q19	1MHz select- Normally masked – used only during Cscape Override.
%Q20	Asynchronous counter reset. Keep low for normal operation. Normally masked– used only during Cscape Override.
%Q21-24	Not used.
%Q25-32	Outputs 1-8 polarities- Normally masked–used only during Cscape Override.
%Q33-34	Input voltage select- Normally masked – used only during Cscape Override.
%Q35-36	Input filter select- Normally masked – used only during Cscape Override.
%Q37	Prescaler select 0- Normally masked – used only during Cscape Override.
%Q38	Prescaler select 1- Normally masked – used only during Cscape Override
%Q39-40	Not used.
%AI1 WORD	Option number for configuration verification 3 (Option number)
%AI2 WORD	Counter A value low word
%AI3 WORD	Counter A value high word
%AQ1 DWORD	Low time 1 low word
%AQ2	Low time 1 high word
%AQ3 DWORD	High time 1 low word
%AQ4	High time 1 high word
%AQ5 DWORD	Low time 2 low word
%AQ6	Low time 2 high word
%AQ7 DWORD	High time 2 low word
%AQ8	High time 2 high word
%AQ9 DWORD	Low time 3 low word
%AQ10	Low time 3 high word
%AQ11 DWORD	High time 3 low word
%AQ12	High time 3 high word
%AQ13 DWORD	Low time 4 low word
%AQ14	Low time 4 high word
%AQ15 DWORD	High time 4 low word
%AQ16	High time 4 high word
%AQ17 DWORD	Low time 5 low word
%AQ18	Low time 5 high word
%AQ19 DWORD	High time 5 low word
%AQ20	High time 5 high word

%AQ21 DWORD	Low time 6 low word
%AQ22	Low time 6 high word
%AQ23 DWORD	High time 6 low word
%AQ24	High time 6 high word
%AQ25 DWORD	Low time 7 low word
%AQ26	Low time 7 high word
%AQ27 DWORD	High time 7 low word
%AQ28	High time 7 high word
%AQ29 DWORD	Low time 8 low word
%AQ30	Low time 8 high word
%AQ31 DWORD	High time 8 low word
%AQ32	High time 8 high word
%AQ33 DWORD	Counts per revolution low word
%AQ34	Counts per revolution high word

5.3 Direct I/O Function

In the Direct I/O function, the read and write registers are directly accessible as outputs are turned ON and OFF. Eight %I and seven %Q registers are used in the Direct I/O function. %Q8 is the MASK (or override bit), which overrides the Cscape setup if it is set to 1.

Note: An output is only available if the associated cam signal has been merged into another output.

%I and %Q registers are connected to the input and output pins of connector J3. The values in the %I registers can be measured at the input pins, and the values in the %Q registers can be measured at the output pins.

A read of the %I registers returns the eight input pins, and a write to the %Q registers latches data to seven lines of the output pin multiplexer. Between one and eight of the output pins can be preempted by cam output signals. The remaining outputs are available as general purpose outputs. The read of the %I registers returns the value of the input pins regardless of the configuration.

Table 5.3 – Direct I/O Registers and Pinout

Register	Signal	Input and Output Pins (J3)
%I1	Input1	1
%I2	Input2	2
%I3	Input3	3
%I4	Input4	4
%I5	Input5	5
%I6	Input6	6
%I7	Input7	7
%I8	Input8	8
%Q1	Output1	10
%Q2	Output2	11
%Q3	Output3	12
%Q4	Output4	13
%Q5	Output5	14
%Q6	Output6	15
%Q7	Output7	16
%Q8	MASK or Cscape Override Bit. Leave at 0 to preserve the Cscape setup.	17

5.4 I/O Map

The I/O Map shows the functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.

The register blocks that are shown in white are normally accessible using the ladder code. The OCS/RCS has a ladder program that the user sets parameters for. If the user does not set parameters for any one of these blocks, the OCS/RCS automatically writes a zero into the block.

The register blocks that are shown in light gray are automatically configured by Cscape if %Q8 (the MASK or override bit) is set to 0. This is the normal setup for most applications. However, in dynamic applications that require parameter changes during runtime, the light gray blocks can be overridden. Refer to the final section in Chapter One, which covers Cscape Override procedures. If Cscape Override procedures are used, %Q8 is set to 1.

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes during runtime.

The dark gray blocks are not used.

Table 5.4 – I/O Map

%I	0	1	2	3	4	5	6	7	8	9
%I 0x		Input1	Input2	Input3	Input4	Input5	Input6	Input7	Input8	Out 1
%I 1x	Out 2	Out 3	Out 4	Out 5	Out 6	Out 7	Out 8			
%Q	0	1	2	3	4	5	6	7	8	9
%Q 0x		Out 1	Out 2	Out 3	Out 4	Out 5	Out 6	Out 7	MASK	Mrg1
%Q 1x	Mrg2	Mrg3	Mrg4	Mrg5	Mrg6	Mrg7		MPOL	MPHS	1MHz
%Q 2x	Reset					POL 1	POL 2	POL 3	POL 4	POL 5
%Q 3x	POL 6	POL 7	POL 8	V-in	V-in	Freq-in	Freq-in	PS 0	PS 1	
%Q 4x										
Not used						Masked if MASK (%Q8) is not set.				

%AI1 WORD	3 (Option number)
%AI2 WORD	Counter A value low
%AI3 WORD	Counter A value high
%AQ1 DWORD	Low time 1 low word
%AQ2	Low time 1 high word
%AQ3 DWORD	High time 1 low word
%AQ4	High time 1 high word
%AQ5 DWORD	Low time 2 low word
%AQ6	Low time 2 high word
%AQ7 DWORD	High time 2 low word
%AQ8	High time 2 high word
%AQ9 DWORD	Low time 3 low word
%AQ10	Low time 3 high word
%AQ11 DWORD	High time 3 low word
%AQ12	High time 3 high word
%AQ13 DWORD	Low time 4 low word
%AQ14	Low time 4 high word
%AQ15 DWORD	High time 4 low word
%AQ16	High time 4 high word
%AQ17 DWORD	Low time 5 low word
%AQ18	Low time 5 high word
%AQ19 DWORD	High time 5 low word
%AQ20	High time 5 high word
%AQ21 DWORD	Low time 6 low word
%AQ22	Low time 6 high word
%AQ23 DWORD	High time 6 low word
%AQ24	High time 6 high word
%AQ25 DWORD	Low time 7 low word
%AQ26	Low time 7 high word
%AQ27 DWORD	High time 7 low word
%AQ28	High time 7 high word
%AQ29 DWORD	Low time 8 low word
%AQ30	Low time 8 high word
%AQ31 DWORD	High time 8 low word
%AQ32	High time 8 high word
%AQ33 DWORD	Counts per revolution low word
%AQ34	Counts per revolution high word

Note: This table serves as a general reference for the starting location of the registers. To determine the *actual* starting location of the various registers, it is necessary to consult the "I/O Map" screen in the Cscape Software *after* configuration. Refer to the following Configuration Procedures in this chapter for more details.

5.5 Option 3 Configuration Procedures

1. After performing the initial configuration procedures described in Chapter Two, the following screen appears (Figure 5.10): Select Option 3 and press **Configure**.

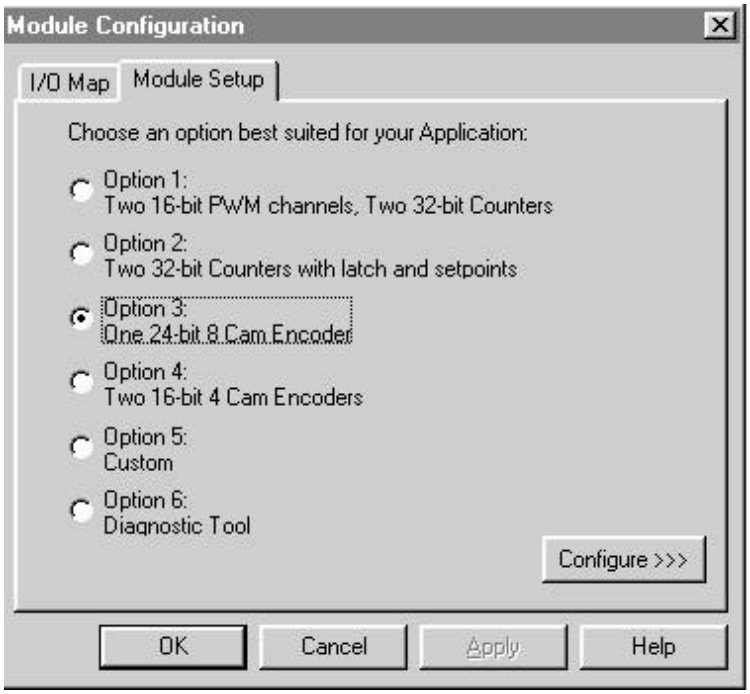


Figure 5.10 – Option 3 Configuration Screen

2. The following screen appears (Figure 5.11):

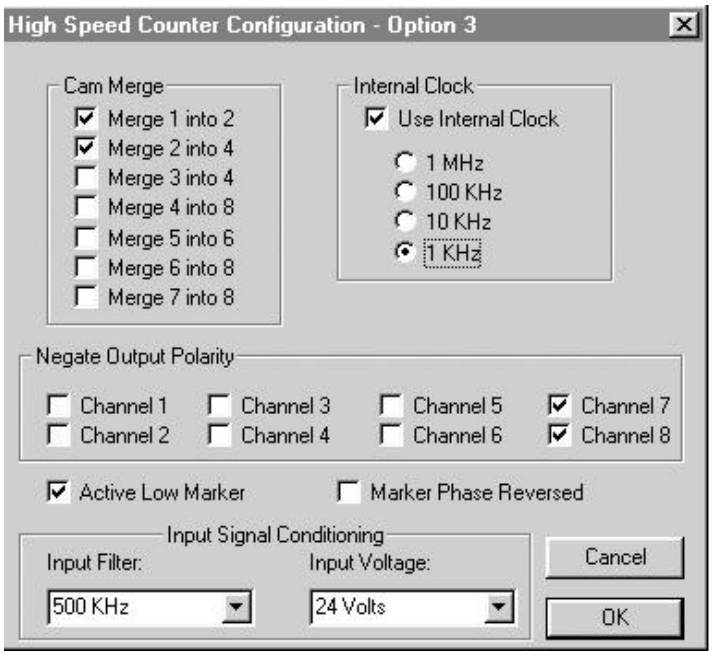


Figure 5.11 – Option 3 Configuration Screen

3. If desired, outputs can be merged in various combinations to allow multiple ON/OFF events to occur per revolution for a given output. Cscape merge combinations are listed on the Option 3 screen. In this example, four ON/OFF events have been merged and are output via Channel Four.

Note: When merging events, the output channel is the highest channel number.

Note: If different merge combinations are desired *during runtime* than those listed on Option 3's screen, see the Cscape Override Configuration Procedures located in Section 5.6.

4. If use of the internal clock is desired, click the box labeled **Use Internal Clock**. Then, click the circle next to the desired clock output.

5. If the **Negate Polarity Output** circuit is used for any of the eight channels, click on the box next to the appropriate channel. (The Negate Polarity Output circuit reverses the polarity of the normal ON/OFF setpoints. For example, the ON setpoint is normally LO, but if the Negate Polarity Output is selected for the channel, the ON setpoint becomes a HI.)

6. If desired, click the appropriate boxes labeled Active Low Marker or Marker Phase Reversed.

7. The **Input Signal Conditioning** block allows the user to set the input voltage threshold and the input frequency response for noise filtering. It is located on the lower left side of the configuration screen. (See Figure 5.11.) Using the corresponding pull-down menus, select the input voltage and the input frequency for noise filtering.

Note: If different threshold and filtering levels are desired *during runtime* than those listed on the Option 3 configuration screen, the user can modify the Cscape parameters using the Advanced Use –Cscape Override Procedures in Section 5.6. The Cscape Override procedures are <u>not</u> intended for most applications and are recommended only for applications that require parameter changes *during runtime.*

8. After selections are made, press **OK**.

9. The **Module Configuration** screen appears. Select the **I/O Map** tab. The I/O Map shows the number of registers and the starting location of the registers. (See Figure 5.12)

Note: For this configuration example, the I/O Map information shown is not necessarily a true representation of the registers and the starting locations. *It is important to understand how to read the information in the registers for an actual setup*.

Example: If the %I starting location = 10, then what is referred to as %I1 (in this chapter) is really %I10 in the actual I/O Map.

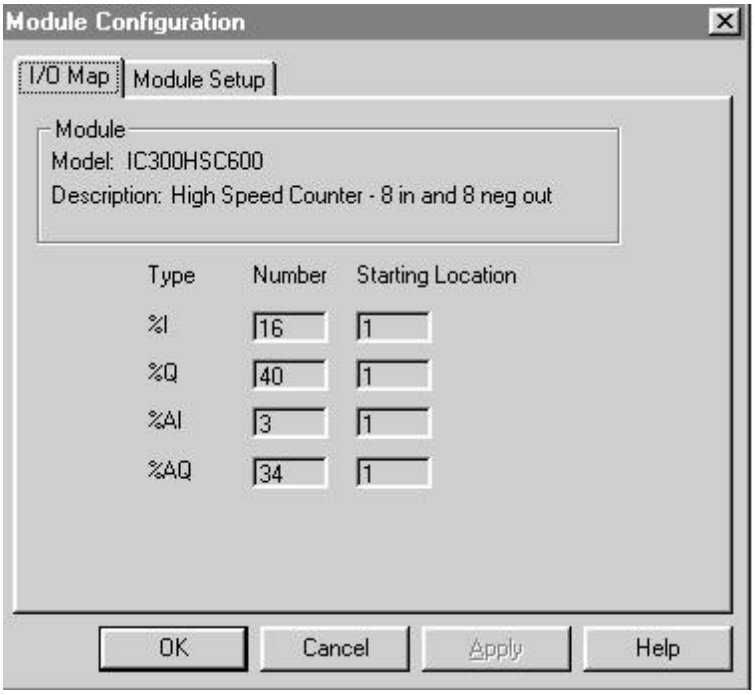


Figure 5.12 – "I/O Map" Tab Selected

5.6 Advanced Use – Cscape Override Procedures

5.6.1 General

Most application requirements are met using the standard Cscape configuration procedures described earlier in this chapter. The user sets parameters using the Cscape Configuration screen, and the Cscape program has exclusive control over the application at all times. The parameters remain the same (or static) during runtime, and they do not change unless the user reconfigures the setup.

However, there are some applications where it may be necessary to override the Cscape configuration setup during runtime. The HSC600/601 gives the user the flexibility of writing a ladder code program to allow changes to the Cscape parameters during runtime. Such applications are dynamic in that the parameters change when the program is executing. Note that the Cscape configuration is used during power-up and continues until the program overrides the configuration.

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes during runtime.

5.6.2 Overriding Cscape Parameters using a Ladder Code Program

Note: If the user intends to change one or more registers using Cscape Override Procedures, ALL registers must be configured from the ladder code as specified in the Cscape Override section for that each option.

A ladder code program must be written to allow the override of the Cscape configuration during runtime. The programmer needs to manually set values into many of the registers that Cscape normally configures.

Although the ladder code program is used during runtime to override the Cscape setup, the standard Cscape configuration procedures must still be performed in order to download the necessary parameters required by the OCS/RCS for power-up. At runtime, the ladder program assumes control and overrides the Cscape configuration parameters.

The following registers need to be manually set using the ladder code program that is written to override the Cscape configuration.

1. Set %Q8 to 1 to override the Cscape configuration of the counter clock source, marker conditioning, output merge selection, and input signal conditioning.

Table 5.5 – OCS/RCS Registers	
Register	**Description**
%Q8	Set to 1.

a. <u>To override Marker Conditioning and Counter Clock Source</u>

The marker polarity is configured using the %Q17 register. Set it to one for an active low marker.

The marker phase is configured using the %Q18 register. Set it to one if the marker is synchronized to the low phase of the B input.

The counter clock source is configured using the %Q19 register. Setting Q19 high uses the 1 MHz internal clock source and forces the UP counting mode. Setting Q19 low uses the **A quad B** inputs to clock the counter.

The following tables describe the relationship of these %Q values and the resulting configuration.

Table 5.6 - Marker Conditioning and Counter Clock Source			
%Q17	**%Q18**	**%Q19**	**Mode**
0			Active high marker
1			Active low marker
	0		Marker during B high
	1		Marker during B low
		0	A quad B
		1	Internal Clock

Table 5.7 – Internal Clock		
%Q29	**%Q30**	**Clock Output**
0	0	1 MHz
1	0	100 KHz
0	1	10 KHz
1	1	1 KHz

b. To override Output Merge Selection

%Q9 through %Q15 are the seven output merge registers. Each one is associated with one cam signal. When it is set to one, the associated cam signal is disconnected from its output pin and merged with another cam signal. If one cam signal is merged with a second and the second is merged with a third, then all three signals appear at the third's output pin and the output pins associate with the first two may be used as general purpose outputs. Up to eight cam signals may be merged in this way into one output. All combinations of merge register values are valid. Cam signal 8 is always connected to output pin 8. The following table describes the function of each merge register.

Table 5.8 - Output Merge Registers			
%Q	**Cam #**	**Level**	**Function**
%Q9	1	0	Connect cam signal 1 to output 1
%Q9	1	1	Merge cam signal 1 with cam signal 2
%Q10	2	0	Connect cam signal 2 to output 2
%Q10	2	1	Merge cam signal 2 with cam signal 4
%Q11	3	0	Connect cam signal 3 to output 3
%Q11	3	1	Merge cam signal 3 with cam signal 4
%Q12	4	0	Connect cam signal 4 to output 4
%Q12	4	1	Merge cam signal 4 with cam signal 8
%Q13	5	0	Connect cam signal 5 to output 5
%Q13	5	1	Merge cam signal 5 with cam signal 6
%Q14	6	0	Connect cam signal 6 to output 6
%Q14	6	1	Merge cam signal 6 with cam signal 8
%Q15	7	0	Connect cam signal 7 to output 7
%Q15	7	1	Merge cam signal 7 with cam signal 8
Note that various combinations of 1 through 8 pulses per revolution can be created using the merge registers.			

Example 1.

%AQ9	%AQ10	%AQ11	%AQ12	%AQ13	%AQ14	%AQ15
0	0	0	0	0	0	0

Each cam signal, 1 through 8 is connected to the corresponding output pin. No general purpose outputs.

Example 2.

%AQ9	%AQ10	%AQ11	%AQ12	%AQ13	%AQ14	%AQ15
0	1	1	0	1	1	1

Single pulse on output 1 using cam 1. General purpose output on outputs 2 and 3 (%Q2 and %Q3). Triple pulse on output 4 using cams 2, 3, and 4. General purpose output on outputs 5, 6, and 7 (%Q5, %Q6, and %Q7). Four pulses on output 8 using cams 5, 6, 7, and 8.

Example 3.

%AQ9	%AQ10	%AQ11	%AQ12	%AQ13	%AQ14	%AQ15
1	0	1	0	1	0	1

General purpose output on outputs 1, 3, 5, and 7 (%Q1, %Q3, %Q5, and %Q7). Double pulse on output 2 using cams 1 and 2. Double pulse on output 4 using cams 3 and 4. Double pulse on output 6 using cams 5 and 6. Double pulse on output 8 using cams 7 and 8.

Example 4.

%AQ9	%AQ10	%AQ11	%AQ12	%AQ13	%AQ14	%AQ15
1	1	1	1	1	1	1

General purpose output on outputs 1 through 7 (%Q1 through %Q7). Eight pulses on output 8 per revolution using all eight cam signals.

c. To override the Input Signal Conditioning

The input signal conditioning selected in Cscape may be modified by the ladder program if %Q8 is set. %Q25 and %Q26 control the input threshold and %Q27 and %Q28 control the noise filter.

Table 5.9 - Override of Input Signal Conditioning

%Q26	%Q25	Input Threshold
0	0	12 VDC for 24 volt systems.
0	1	6 VDC for 12 volt systems
1	0	1.4 VDC for TTL compatibility
1	1	0 VDC for AC coupled signals
%Q28	**%Q27**	Noise filter / Maximum operating frequency
0	0	High frequency / 1MHz
0	1	Medium frequency / 100KHz
1	X	Low frequency / 10KHz

CHAPTER 6: OPTION 4

Dual 16-Bit Electronic Cam with Four Combinable ON and OFF Functions per Cam.

6.1 Option 4 Overview

6.1.1 General

Initial configuration procedures to select Option 4 are contained in Chapter Two. The following topics pertaining to Option 4 are covered in Chapter Six:

a. Functions and capabilities; pin-out
b. Registers
c. I/O Map - shows functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.
d. Configuration procedures
e. Advanced Use-Cscape Override Configuration Procedures – used only for applications needing to override the Cscape setup during runtime. Not used in most applications.

6.1.2 Functions

Option 4 gives the HSC600/601 the capabilities to:

a. Operate as Dual 16-Bit Electronic Cam with Four Combinable ON and OFF Functions per Cam.

b. Allow Direct I/O Access: Eight %I and seven %Q registers are directly accessible in the %I and %Q registers of the Operator Control Station (OCS/RCS).

6.1.3 Safety Warning

Warning: Failure to disable the High Speed Counter Module (HSC600/601) manually through the ladder code program could cause either personal injury or damage to equipment.

When the OCS/RCS is in the Idle or Stop modes, the HSC600/601 continues normal operation. **The user must physically disable the HSC600/601 through the ladder code program.**

6.2 Electronic Cam Function

6.2.1 Cam Operation

Option 4 provides *two* electronic cams that are able to control up to four ON/OFF events per cam. Both cams can be merged together allowing control of eight ON/OFF events. (Merges are covered in the following explanation.) Each of the electronic cams consists of a 16-bit counter that can be programmed for any number of total counts per revolution up to 65,535. The following explanation provides a general overview of cam operation using an encoder. (See Figure 6.1.)

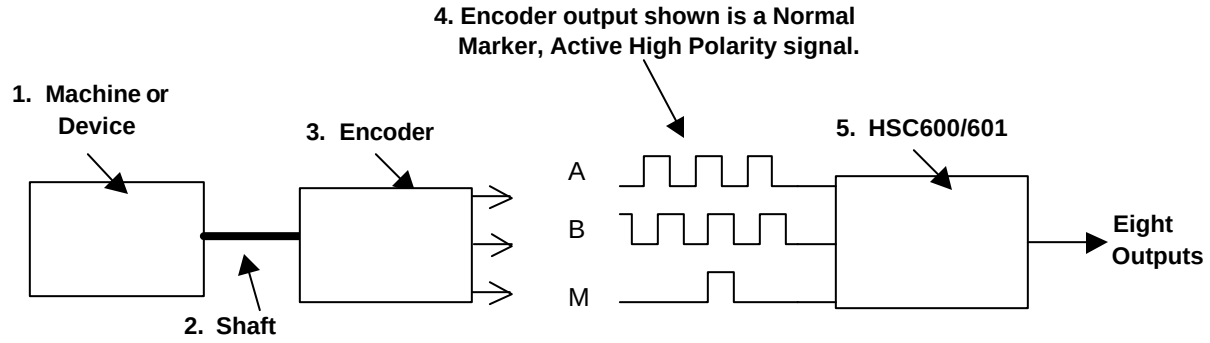


Figure 6.1 – General Overview of Cam Operation using an Encoder (Drawing Not to Scale)

1. A **machine** or other device causes a shaft to rotate.

2. The **shaft** is connected to an encoder. An encoder is a device used to determine the position of a motor as well as the direction and distance that the motor has moved.

3. The **encoder** sends outputs to the HSC600/601 that are in a specific format depending upon the encoder used. (The user needs to consult the encoder manufacturer's manual to determine the encoder's output format.) In order to properly configure the HSC600/601, it is necessary to know the type of signals that the encoder is sending to it.

4. Typical **encoder output signals** are depicted in Figures 6.1 – 6.8. The HSC600/601 cam counter is normally driven by a **A quad B** quadrature signal from a rotary encoder. Quadrature outputs consist of A and B signals as well as a marker signal. Signal A needs to be 90° in or out-of phase with the Signal B. The marker signal represents zero as the encoder completes a revolution. The marker signal must always be in sync with the B signal, but the polarities can differ.

The encoder output signal shown in **Figure 6.1 (and Figure 6.2**) is a Normal Marker with active high polarity. This means that the marker is synced with Signal B and has a positive polarity when Signal B is high. The user must know the characteristics of the encoder output signal in order to properly configure the HSC600/601.

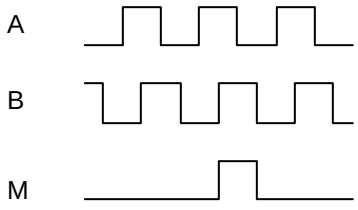


Figure 6.2 – Normal Marker, Active High Polarity

Interpretation of Other Encoder Ouput Signals:

With A quad B signals, the counter increments on each edge, i.e. 4X mode. In **Figure 6.3,** the interpretation of the A and B phase is such that a rising edge on A with B low is an UP count. (Signal A leads B by 90°.) In **Figure 6.4**, the interpretation of the A and B phase is such that a falling edge on A with B low is a DOWN count. (Signal B leads Signal A by 90°.) This describes just one of the four counts per encoder A-B cycle.

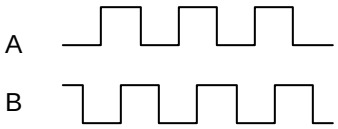


Figure 6.3 - Count UP (4x)

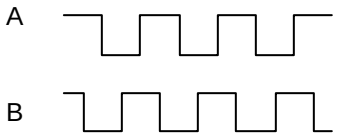


Figure 6.4 - Count DOWN (4x)

In **Figure 6.5**, the marker is active high and 180° out-of-phase with Signal B. In **Figure 6.6**, the marker is inverted active low and is in phase with Signal B. In **Figure 6.7**, the marker is active low and 180° out-of-phase with Signal B.

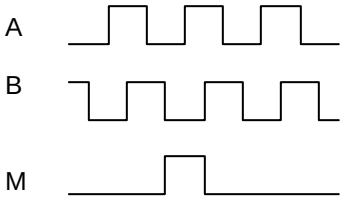


Figure 6.5 – Reverse Phase Marker, Active High Polarity

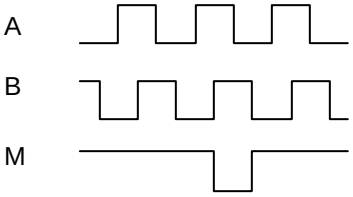


Figure 6.6 – Normal Marker, Active Low Polarity

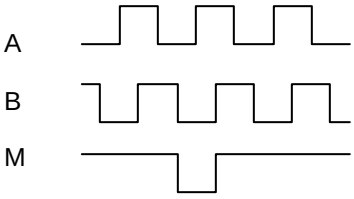
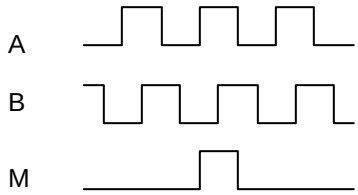


Figure 6.7 – Reverse Phase Marker, Active Low Polarity



Note: Swap A and B channels at connector and rename them so that the marker is synchronized with the new B channel.

Figure 6.8 – Marker Synchronized with Channel A

In **Figure 6.8**, the marker logic expects the marker to be synchronized with the B input so that there is only one A edge during the marker active interval. If the marker is synchronized with the nominal A channel on the encoder, exchange the A and B channels at the connector.

5. In Option 4, the **HSC600/601** acts as two electronic cams, which are able to control up to four ON/OFF events per cam. (Both cams can be merged together allowing control of eight ON/OFF events.) ON/OFF events are caused electronically. Examples of ON/OFF events include turning a motor or a switch on and off. The following aspects of cam operation are necessary to understand in order to properly configure the HSC600/601.

Set-points

There are four cam lobe switches per cam within the HSC600/601, and each switch has a separately programmed ON count and OFF count. The ON and OFF counts are referred to as set-point values. There are high and low set-point values, which are determined by the user. Events can be programmed to occur when the ON/OFF set-point values are reached during counting. See more information on set-points and %AQ Registers, see Section 6.2.5 and Section 6.4 (Table 6.4).

Merging Outputs – Combining Events

The outputs can be merged in various combinations for multiple on/off cycles per revolution for a given output. The merge is configured using the Cscape Software or by using the Cscape Override Configuration Procedures located in Section 6.6.

Each switch is normally connected to a separate output pin so that there is one ON/OFF event for each of the output channels. (In Option 4, there are four output channels per cam.) However, it also possible to configure the HSC600/601 so that the outputs are merged in various combinations for multiple pulse per revolution functions. A *maximum* of four ON/OFF events (per cam) can be merged in the HSC600/601 using Option 4. Both cams can be merged together allowing *maximum* control of eight ON/OFF events.

Proper Configuration of Input Signals from the Encoder

When configuring the HSC600/601 in Option 4, the marker polarity and phase can be programmed to match a particular encoder format. **(See Figure 6.9.)** The counter total count is normally set to the same number of counts as the encoder resolution but can be set to a higher number for multi-revolution applications such as for a linear cam. In this case the encoder marker should be masked for all revolutions (using marker disable) except for the home section by keeping the marker disable input high while out of the home section. The marker disable input should be tied low for normal operation. Marker and marker disable inputs are provided in the HSC600/601.

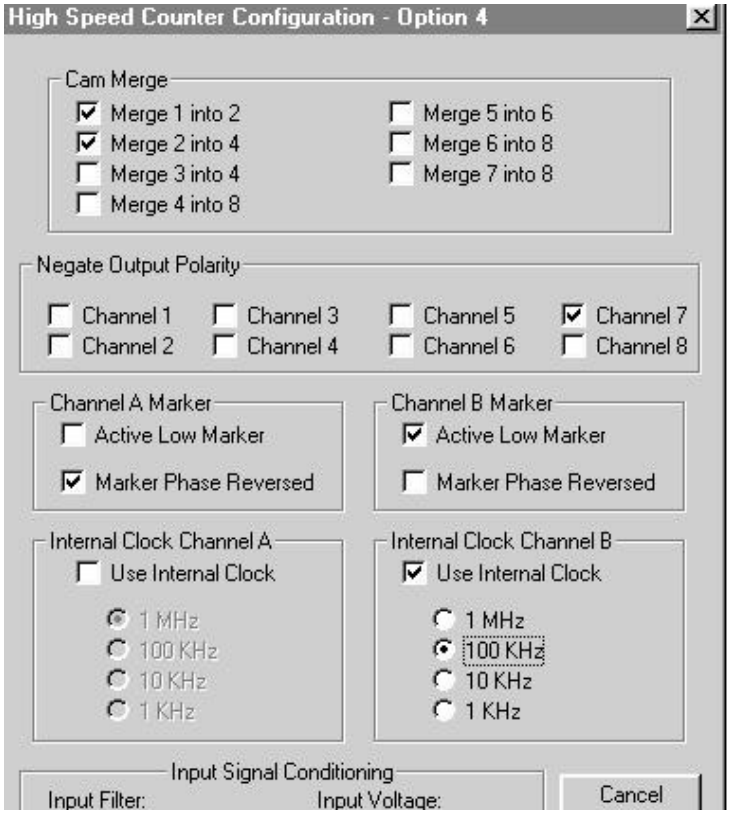


Figure 6.9 – Option 4 Configuration Screen

The marker phase may be specified to support encoders with the marker channel synchronized to the low phase or the high phase of the B input. The marker polarity may be specified to support encoders with active high or active low marker outputs.

Internal Clock (Used for Time-Based Applications)

If an encoder is not used, the counter can be clocked by an internal selectable, programmable clock signal to create a flexible electronic pulse / timing generator with up to1µs resolution with a programmable repeat time of up to four hours. An asynchronous reset is provided using the %Q20 register. Write a zero to this register for normal operation. See Section 6.2.5 (Table 6.2).

Advanced Use – Cscape Override Procedures

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes *during runtime*.

The marker configuration, counter clock source, and output merges are configured by Cscape. If the mask bit, %Q8, is set to 1, the Cscape configuration is overridden by Registers %Q9 through %Q28. (See the Cscape Override Configuration Procedures located in **Section 6.6**.) Each of the cam ON and OFF times and the number of counts per revolution are set using DWORD %AQ registers.

6.2.2 Set-points

There are four cam lobe switches per cam within the HSC600/601, and each switch has a separately programmed ON count and OFF count. The ON and OFF counts are referred to as set-point values. There are high and low set-point values, which are determined by the user. Events can be programmed to occur when the ON/OFF set-point values are reached during counting

Normally, the ON time uses the high set-point, and the OFF time uses the low set-point. However if required, the user can configure the HSC600/601 to invert the set-point values by marking the **Negate Output Polarity** block on the Option 3 configuration screen.

Each set-point pair defines a count range (bracketed by the low and high set-points) in which the cam signal is active. For proper operation, the high set-point is always numerically higher than the low set-point. If the maximum count is less than the high set-point, the maximum count becomes the high set-point. If the maximum count is less than the low set-point, the cam signal never becomes active. The output polarity selection in Cscape defines whether the active range is on / positive polarity or off / negative polarity. Refer to Section 6.4 (Table 6.4) for information on %AQ registers.

The example below uses a low set-point of 200 and a high set-point of 400.

COUNT	POLARITY	OUTPUT
100	POSITIVE	OFF
300	POSITIVE	ON
500	POSITIVE	OFF
100	NEGATIVE	ON
300	NEGATIVE	OFF
500	NEGATIVE	ON

6.2.3 Connector

Table 6.1 lists the A and B signals, M, M disable inputs, and cam signal outputs.

Table 6.1 – Option 4 Pin-out

Name	Input1	Input2	Input3	Input4	Input5	Input6	Input7	Input8
Pin	1	2	3	4	5	6	7	8
Use	A(A)	B(A)	M(A)	M(A) disable	A(B)	B(B)	M(B)	M(B) disable
Pin	10	11	12	13	14	15	16	17
Use	CAM 1A/ Output 1	CAM 2A/ Output 2	CAM 3A/ Output 3	CAM 4A/ Output 4	CAM 1B/ Output 5	CAM 2B/ Output 6	CAM 3B/ Output 7	CAM 4B
Pin	9	18	19					
Use	Input Common	Output Common	Output Power					

6.2.4 Cam Registers

The registers used by the electronic cam function are defined in Table 6.2. If different parameter levels are desired *during runtime* than those listed on the Option 4 configuration screen, %Q8 (MASK) must be set. (See **Advanced Use –Cscape Override Procedures** in Section 6.6.)

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes *during runtime.*

Note: Table 6.2 depicts *all* registers used in Option 4. **It is important to read through this chapter to obtain information covering different kinds of registers**. Also, the I/O Map (Table 6.4) contains additional information regarding registers used in Option 4.

Table 6.2 – Cam Registers

Registers	Signal
%I1-8	Inputs 1-8
%Q1-7	Outputs 1-7
%Q8	Leave set to 0 to preserve the Cscape configuration setup. This is the MASK (override) bit.
%Q9-15	Merges 1-7. Normally masked-used only during Cscape override.
%Q16	Not used.
%Q17	Channel A marker polarity- Normally masked-used only during Cscape override.
%Q18	Channel A marker phase- Normally masked-used only during Cscape override.
%Q19	Channel A 1MHz select- Normally masked-used only during Cscape override.
%Q20	Asynchronous counter A reset. Keep low for normal operation
%Q21	Channel B marker polarity- Normally masked-used only during Cscape override.
%Q22	Channel B marker phase- Normally masked-used only during Cscape override.
%Q23	Channel B 1MHz select- Normally masked-used only during Cscape override.
%Q24	Asynchronous counter B reset. Keep low for normal operation.
%Q25	Output Polarity 1 - Normally masked-used only during Cscape override.
%Q26	Output Polarity 2 - Normally masked-used only during Cscape override.
%Q27	Output Polarity 3 - Normally masked-used only during Cscape override.
%Q28	Output Polarity 4 - Normally masked-used only during Cscape override.
%Q29	Output Polarity 5 - Normally masked-used only during Cscape override.
%Q30	Output Polarity 6 - Normally masked-used only during Cscape override.
%Q31	Output Polarity 7 - Normally masked-used only during Cscape override.
%Q32	Output Polarity 8 - Normally masked-used only during Cscape override.
%Q33-34	Input voltage select- Normally masked-used only during Cscape override.
%Q35-36	Input filter select- Normally masked-used only during Cscape override.
%Q37	Channel A Prescaler select 0- Normally masked-used only during Cscape override.
%Q38	Channel A Prescaler select 1- Normally masked-used only during Cscape override.
%Q39	Channel B Prescaler select 0- Normally masked-used only during Cscape override.
%Q40	Channel B Prescaler select 1- Normally masked-used only during Cscape override.
%AI1 WORD	Option number for configuration verification
%AI2 WORD	Counter A value
%AI3 WORD	Counter B value
%AQ1 WORD	A Low set-point 1

%AQ2 WORD	A High set-point 1
%AQ3 WORD	A Low set-point 2
%AQ4 WORD	A High set-point 2
%AQ5 WORD	A Low set-point 3
%AQ6 WORD	A High set-point 3
%AQ7 WORD	A Low set-point 4
%AQ8 WORD	A High set-point 4
%AQ9 WORD	B Low set-point 1
%AQ10 WORD	B High set-point 1
%AQ11 WORD	B Low set-point 2
%AQ12 WORD	B High set-point 2
%AQ13 WORD	B Low set-point 3
%AQ14 WORD	B High set-point 3
%AQ15 WORD	B Low set-point 4
%AQ16 WORD	B High set-point 4
%AQ17 WORD	A Total counts per revolution
%AQ18 WORD	B Total counts per revolution

6.3 Direct I/O

In the Direct I/O function, the read and write registers are directly accessible as outputs are turned ON and OFF. Eight %I and seven %Q registers are used in the Direct I/O function. %Q8 is the MASK (or override bit), which overrides the Cscape setup if it is set to 1.

Note: An output is only available if the associated cam signal has been merged into another output.

%I and %Q registers are connected to the input and output pins of connector J3. The values in the %I registers can be measured at the input pins, and the values in the %Q registers can be measured at the output pins. A read of the %I registers returns the eight input pins, and a write to the %Q registers latches data to seven lines of the output pin multiplexer. Between one and eight of the output pins can be preempted by cam output signals. The remaining outputs are available as general purpose outputs. The read of the %I registers returns the value of the input pins regardless of the configuration.

Table 6.3 – Direct I/O Registers and Pinout

Register	Signal	Input and Output Pins (J3)
%I1	Input1	1
%I2	Input2	2
%I3	Input3	3
%I4	Input4	4
%I5	Input5	5
%I6	Input6	6
%I7	Input7	7
%I8	Input8	8
%Q1	Output1	10
%Q2	Output2	11
%Q3	Output3	12
%Q4	Output4	13
%Q5	Output5	14
%Q6	Output6	15
%Q7	Output7	16
%Q8	MASK or Override Bit. Leave at 0 to preserve the Cscape Setup.	17

6.4 I/O Map

Table 6.4 – I/O Map

%I	0	1	2	3	4	5	6	7	8	9
%I 0x		Input1	Input2	Input3	Input4	Input5	Input6	Input7	Input8	

%Q	0	1	2	3	4	5	6	7	8	9
%Q 0x		Out 1	Out 2	Out 3	Out 4	Out 5	Out 6	Out 7	MASK	Mrg1
%Q 1x	Mrg2	Mrg3	Mrg4	Mrg5	Mrg6	Mrg7		MPOL A	MPHS A	1MHz A
%Q 2x	Reset A	MPOL B	MPHS B	1MHz B	Reset B	POL 1	POL 2	POL 3	POL 4	POL 5
%Q 3x	POL 6	POL 7	POL 8	V-in	V-in	Freq-in	Freq-in	PS 0 A	PS 1 A	PS 0 B
%Q 4x	PS 1 B									
Not used						Masked if MASK (%Q8) is not set.				

%AI1 WORD		Option number for configuration verification 3 (Option number)
%AI2 WORD		Counter A value
%AI3 WORD		Counter B value
%AQ1	WORD	A Low time 1
%AQ2	WORD	A High time 1
%AQ3	WORD	A Low time 2
%AQ4	WORD	A High time 2
%AQ5	WORD	A Low time 3
%AQ6	WORD	A High time 3
%AQ7	WORD	A Low time 4
%AQ8	WORD	A High time 4
%AQ9	WORD	B Low time 5
%AQ10	WORD	B High time 5
%AQ11	WORD	B Low time 6
%AQ12	WORD	B High time 6
%AQ13	WORD	B Low time 7
%AQ14	WORD	B High time 7
%AQ15	WORD	B Low time 8
%AQ16	WORD	B High time 8
%AQ17	WORD	A Counts per revolution
%AQ18	WORD	B Counts per revolution

Note: This table serves as a general reference for the starting location of the registers. To determine the *actual* starting location of the various registers, it is necessary to consult the "I/O Map" screen in the Cscape Software *after* configuration. Refer to the following Configuration Procedures in this chapter for more details.

6.5 Option 4 Configuration Procedures

1. After performing the initial configuration procedures described in Chapter Two, the following screen appears (Figure 6.10): Select Option 4 and press **Configure**.

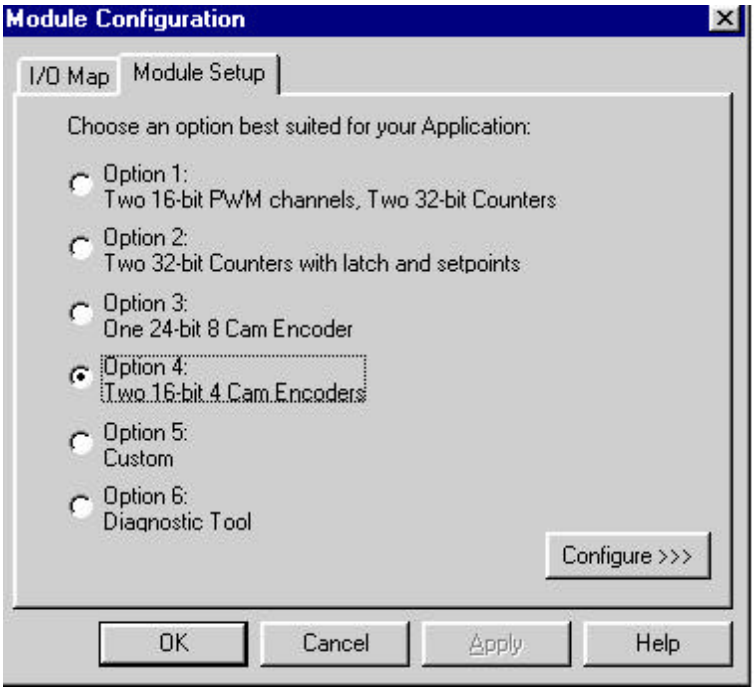


Figure 6.10 – Option 4 Configuration Screen

2. The following screen appears (Figure 6.11):

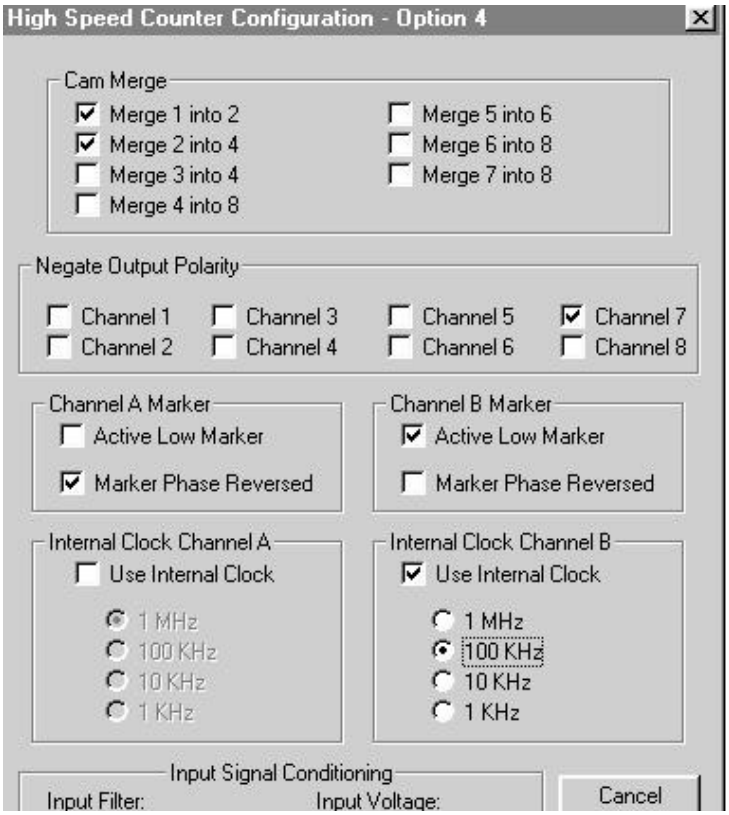


Figure 6.11 – Option 4 Configuration Screen

3. If desired, outputs can be merged in various combinations to allow multiple ON/OFF events to occur per revolution for a given output. Cscape merge combinations are listed on the Option 4 screen.

Note: If different merge combinations are desired *during runtime* than those listed on Option 4's screen, see the Cscape Override Configuration Procedures located in Section 6.6.

4. If use of the internal clock is desired, click the box labeled **Use Internal Clock**. Then, click the circle next to the desired clock output.

5. If the **Negate Polarity Output** circuit is used for any of the eight channels, click on the box next to the appropriate channel. (The Negate Polarity Output circuit reverses the polarity of the normal ON/OFF set-points. For example, the ON set-point is normally LO, but if the Negate Polarity Output is selected for the channel, the ON set-point becomes a HI.)

6. If desired, click the appropriate boxes labeled Active Low Marker or Marker Phase Reversed.

7. The **Input Signal Conditioning** block allows the user to set the input voltage threshold and the input frequency response for noise filtering. It is located on the lower left side of the configuration screen. (See Figure 6.2.) Using the corresponding pull-down menus, select the input voltage and the input frequency for noise filtering.

Note: If different threshold and filtering levels are desired *during runtime* than those listed on the Option 4 configuration screen, the user can modify the Cscape parameters using **the Advanced Use –Cscape Override Procedures** in Section 6.6. The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes *during runtime.*

8. After selections are made, press **OK**.

9. The **Module Configuration** screen appears. Select the **I/O Map** tab. The I/O Map shows the number of registers and the starting location of the registers. (See Figure 6.12.)

Note: For this configuration example, the I/O Map information shown is not necessarily a true representation of the registers and the starting locations. *It is important to understand how to read the information in the registers for an actual setup*.

Example: If the %I starting location = 10, then what is referred to as %I1 (in this chapter) is really %I10 in the actual I/O Map.

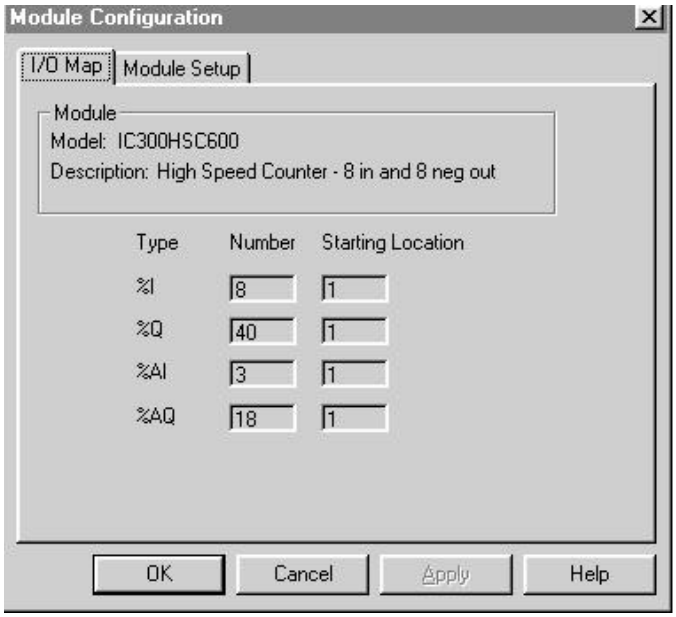


Figure 6.12 – I/O Map Screen

6.6 Advanced Use – Cscape Override Procedures

6.6.1 General

Most application requirements are met using the standard Cscape configuration procedures described earlier in this chapter. The user sets parameters using the Cscape Configuration screen, and the Cscape program has exclusive control over the application at all times. The parameters remain the same (or static) during runtime, and they do not change unless the user reconfigures the setup.

However, there are some applications where it may be necessary to override the Cscape configuration setup during runtime. The HSC600/601 gives the user the flexibility of writing a ladder code program to allow changes to the Cscape parameters during runtime. Such applications are dynamic in that the parameters change when the program is executing. Note that the Cscape configuration is used during power-up and continues until the program overrides the configuration.

Note: The Cscape Override procedures are <u>not</u> intended for most applications and are recommended only for applications that require parameter changes during runtime.

6.6.2 Overriding Cscape Parameters using a Ladder Code Program

Note: If the user intends to change one or more registers using Cscape Override Procedures, ALL registers must be configured from the ladder code as specified in the Cscape Override section for that option.

A ladder code program must be written to allow the override of the Cscape configuration during runtime. The programmer needs to manually set values into many of the registers that Cscape normally configures.

Although the ladder code program is used during runtime to override the Cscape setup, the standard Cscape configuration procedures must still be performed in order to download the necessary parameters required by the OCS/RCS for power-up. At runtime, the ladder program assumes control and overrides the Cscape configuration parameters.

The following registers need to be manually set using the ladder code program that is written to override the Cscape configuration.

1. Set %Q8 to 1 to override the Cscape configuration of the counter clock source, marker conditioning, output merge selection, and input signal conditioning.

Table 6.5 – OCS/RCS Registers	
Register	**Description**
%Q8	Set to 1.

<u>a. To override Marker Conditioning and Counter Clock Source</u>

The marker polarity is configured using the %Q17 / %Q21 registers. Set it to one for an active low marker.

The marker phase is configured using the %Q18 / %Q22 registers. Set it to one if the marker is synchronized to the low phase of the B input.

The counter clock source is configured using the %Q19 / %Q23 registers. Setting it high uses the 1 MHz internal clock source and forces the up counting mode. Setting it low uses the A quad B inputs to clock the counter.

The following tables describe the relationship of these %Q values and the resulting configuration.

Table 6.6 - Marker Conditioning and Counter Clock Source						
A	B	A	B	A	B	← A / B Counter Reference
%Q17	%Q21	%Q18	%Q22	%Q19	%Q23	Mode
0						Active high marker
1						Active low marker
		0				Marker during B high
		1				Marker during B low
				0		A quad B
				1		1 MHz count up

Table 6.7 – Internal Clock		
%Q29	**%Q30**	**Clock Output**
0	0	1 MHz
1	0	100 KHz
0	1	10 KHz
1	1	1 KHz

b. To override Output Merge Selection

%Q9 through %Q15 are the seven output merge registers. Each one is associated with one cam signal. When it is set to one, the associated cam signal is disconnected from its output pin and merged with another cam signal. If one cam signal is merged with a second and the second is merged with a third, then all three signals appear at the third's output pin and the output pins associate with the first two may be used as general purpose outputs. Up to eight cam signals may be merged in this way into one output. All combinations of merge register values are valid. Cam signal 8 is always connected to output pin 8. The following table describes the function of each merge register.

Table 6.8 – Output Merge Registers			
%Q	Cam #	Level	Function
%Q9	1A	0	Connect cam signal 1A to output 1
%Q9	1A	1	Merge cam signal 1A with cam signal 2A
%Q10	2A	0	Connect cam signal 2A to output 2
%Q10	2A	1	Merge cam signal 2A with cam signal 4A
%Q11	3A	0	Connect cam signal 3A to output 3
%Q11	3A	1	Merge cam signal 3A with cam signal 4A
%Q12	4A	0	Connect cam signal 4A to output 4
%Q12	4A	1	Merge cam signal 4A with cam signal 4B
%Q13	1B	0	Connect cam signal 1B to output 5
%Q13	1B	1	Merge cam signal 1B with cam signal 2B
%Q14	2B	0	Connect cam signal 2B to output 6
%Q14	2B	1	Merge cam signal 2B with cam signal 4B
%Q15	3B	0	Connect cam signal 3B to output 7
%Q15	3B	1	Merge cam signal 3B with cam signal 4B

Note that various combinations of 1 through 8 pulses per revolution on multiple outputs may be created using the merge registers.

Example 1.

%AQ9	%AQ10	%AQ11	%AQ12	%AQ13	%AQ14	%AQ15
0	0	0	0	0	0	0

Each cam signal, 1A through 4B is connected to the corresponding output pin. No general purpose outputs.

Example 2.

%AQ9	%AQ10	%AQ11	%AQ12	%AQ13	%AQ14	%AQ15
0	1	1	0	1	1	1

Single pulse on output 1 using cam 1A. General purpose output on outputs 2 and 3 (%Q2 and %Q3). Triple pulse on output 4 using cams 2A, 3A, and 4A. General purpose output on outputs 5, 6, and 7 (%Q5, %Q6, and %Q7). Four pulses on output 8 using cams 1B, 2B ,3B, and 4B.

Example 3.

%AQ9	%AQ10	%AQ11	%AQ12	%AQ13	%AQ14	%AQ15
1	0	1	0	1	0	1

General purpose output on outputs 1, 3, 5, and 7 (%Q1, %Q3, %Q5, and %Q7). Double pulse on output 2 using cams 1A and 2A. Double pulse on output 4 using cams 3A and 4A. Double pulse on output 6 using cams 1B and 2B. Double pulse on output 8 using cams 3B and 4B.

Example 4.

%AQ9	%AQ10	%AQ11	%AQ12	%AQ13	%AQ14	%AQ15
1	1	1	1	1	1	1

General purpose output on outputs 1 through 7 (%Q1 through %Q7). Eight pulses on output 8 per revolution using all eight cam signals. Note that setting %AQ12 merges outputs from both counters.

c. To override Input Signal Conditioning

The input signal conditioning selected in Cscape can be modified by the ladder program if %Q8 is set. %Q25 and %Q26 control the input threshold and %Q27 and %Q28 control the noise filter.

Table 6.9

%Q26	%Q25	Input Threshold
0	0	12 VDC for 24 volt systems.
0	1	6 VDC for 12 volt systems
1	0	1.4 VDC for TTL compatibility
1	1	0 VDC for AC coupled signals
%Q28	%Q27	Noise filter / Maximum operating frequency
0	0	High frequency / 1MHz
0	1	Medium frequency / 100KHz
1	X	Low frequency / 10KHz

CHAPTER 7: OPTION 5

Field Installable Options

7.1 Option 5 Overview

7.1.1 General

Initial configuration procedures to select Option 5 are contained in Chapter Two. The following topics pertaining to Option 5 are covered in Chapter Seven:

a. Function / Installation of a Custom Option
b. Registers
c. I/O Map - shows functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.
d. Configuration procedures
e. Advanced Use-Cscape Override Configuration Procedures – used only for applications needing to override the Cscape setup during runtime. Not used in most applications.

Note: Be sure to refer to the additional user documentation provided for the new option before configuration.

7.1.2 Safety Warning

Warning: Failure to disable the High Speed Counter Module (HSC600/601) manually through the ladder code program could cause either personal injury or damage to equipment.

When the OCS/RCS is in the "Idle" or "Stop" modes, the HSC600/601 continues normal operation. **The user must physically disable the HSC600/601 through the ladder code program.**

7.2 Function / Installation of a Custom Option

Option 5 allows the field installation of an option that is not included in Cscape's internal set of options. It enables a user to install a new or custom option without having to obtain a new version of Cscape Software.

If an option is desired but unavailable in Cscape, an external option file can be emailed to the user. The user loads the file into any convenient directory and configures the HSC600/601 using Option 5. The user selects input signal conditioning parameters (i.e., input voltage threshold and filtering levels) from pull-down menus on the Option 5 configuration screen. The Cscape program loads the external option file into the OCS/RCS. The option is then installed. Additional user documentation is provided for the new option.

7.3 Registers

7.3.1 System I/O Registers

Table 7.1 lists the predefined registers for system functions. If different threshold and filtering levels are desired *during runtime* than those listed on the Option 5 configuration screen, %Q7 (MASK) must be set. (See **Advanced Use –Cscape Override Procedures** in Section 7.5.)

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes *during runtime.*

See Table 7.3 for additional information regarding all registers used in Option 5.

Table 7.1 – System I/O Registers

Register	Description
%Q1-2	Voltage Input Select – Normally masked-used during Cscape Override.
%Q3-4	Filter Frequency Select-Normally masked-used during Cscape Override
%Q5	Auxiliary 1
%Q6	Auxiliary 2
%Q7	Leave set to 0 to preserve Cscape setup. This is the MASK (override) bit.
%Q8	Not used.
%AI1 WORD	Option number for configuration verification.

7.3.2 Standard I/O Registers

Fifteen %AI and fifteen %AQ registers are available for this option.
See Table 7.3 for additional information regarding all registers used in Option 5.

Table 7.2 – Standard I/O Registers

Register	Description
%AI2 through %AI16	Input registers
%AQ1 through %AQ15	Output registers

7.4 I/O Map

The I/O Map shows the functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.

The register blocks that are shown in white are normally accessible using the ladder code. The user sets the parameters. If the user does not set parameters for any one of these blocks, the OCS/RCS automatically writes a zero into the block.

The register blocks that are shown in light gray are automatically configured by Cscape if %Q7 (the MASK or override bit) is set to 0. This is the normal setup for most applications. However, in dynamic applications that require parameter changes during runtime, the light gray blocks can be overridden if %Q7 is set to **1**.

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes during runtime.

The dark gray blocks are not used.

Table 7.3 – I/O Map

%Q	0	1	2	3	4	5	6	7	8	9
%Q 0x		V-in	V-in	Freq-in	Freq-in	Aux1	Aux2	MASK		
Not used						Masked if MASK (%Q7) is not set.				

%AI1	WORD	5 (Option number)
%AI2	WORD	First user input word
%AI3	WORD	Second user input word
%AI4-15	WORD	Third through fourteenth user input word
%AI16	WORD	Fifteenth user input word
%AQ1	WORD	First user output word
%AQ2-14	WORD	Second through fourteenth user output word
%AQ15	WORD	Fifteenth user output word

Note: This table serves as a general reference for the starting location of the registers. To determine the *actual* starting location of the various registers, it is necessary to consult the "I/O Map" screen in the Cscape Software *after* configuration. Refer to the following Configuration Procedures in this chapter for more details.

7.4 General Configuration Procedures/Loading an External Option File

Note: The following procedures are provided as general guidelines to load an external option file into the OCS/RCS using Cscape Software. Be sure to consult the user documentation that is provided with the external option file before performing the configuration procedures listed below.

1. Upon obtaining an external option file, place it into an appropriate directory.

2. After performing the initial configuration procedures described in Chapter Two, the following screen appears (Figure 7.1): Press **Configure**.

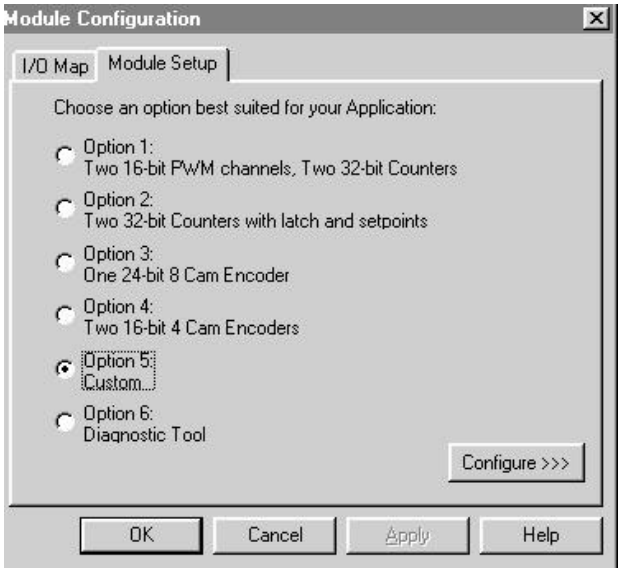


Figure 7.1 – Option 5 Configuration Screen

3. The following screen appears (Figure 7.2): Press **Browse** and locate the external option file. (Another screen appears.) Select the file and press **Open**.

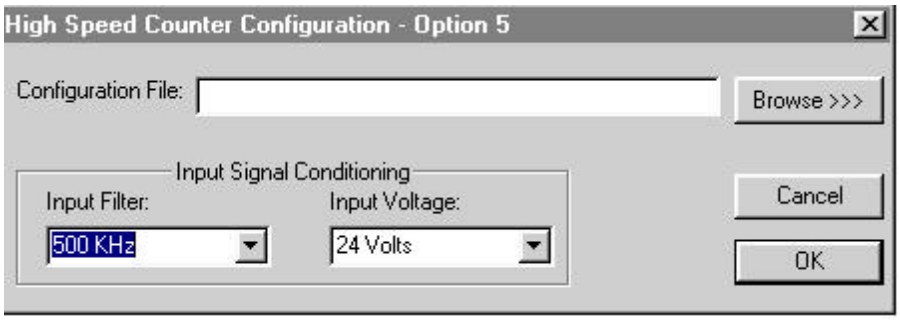


Figure 7.2 – Option 5 Configuration Screen

4. The Option 5 screen re-appears (Figure 7.2):

5. Select a desired voltage threshold and frequency for noise filtering from pull-down menus on the Option 5 screen. Press **OK**.

Note: If different threshold and filtering levels are desired *during runtime* than those listed on the Option 5 configuration screen, the user can modify the Cscape parameters using the **Advanced Use – Cscape Override Procedures** in Section 7.5. The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes *during runtime.*

5. The Cscape program loads the external option file into the OCS/RCS. (This takes a few seconds.) The option is then installed. The following screen appears:

6. Select the **I/O Map** tab. The I/O Map shows the number of registers and the starting location of the registers. (See Figure 7.3.)

Note: For this configuration example, the I/O Map information shown is not necessarily a true representation of the registers and the starting locations. *It is important to understand how to read the information in the registers for an actual setup*.

Example: If the %I starting location = 10, then what is referred to as %I1 (in this chapter) is really %I10 in the actual I/O Map.

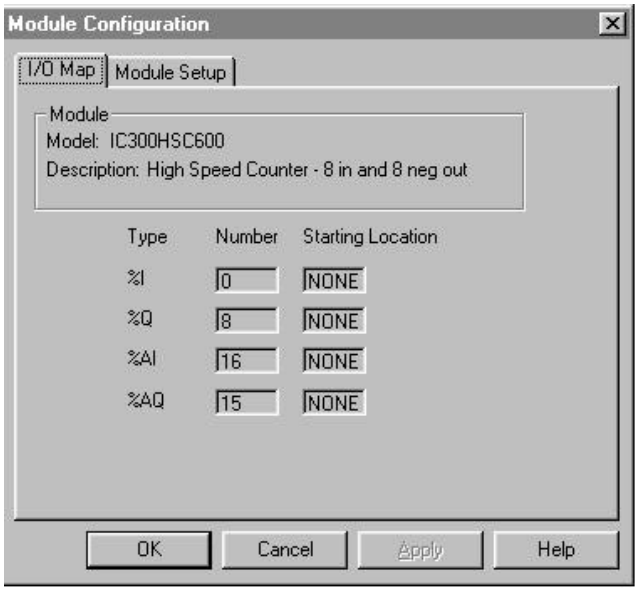


Figure 7.3 – I/O Map Screen

7.5 Advanced Use – Cscape Override Procedures

7.5.1 General

Most application requirements are met using the standard Cscape configuration procedures described earlier in this chapter. The user sets parameters using the Cscape Configuration screen, and the Cscape program has exclusive control over the application at all times. The parameters remain the same (or static) during runtime, and they do not change unless the user reconfigures the setup.

However, there are some applications where it may be necessary to override the Cscape configuration setup during runtime. The HSC600/601 gives the user the flexibility of writing a ladder code program to allow changes to the Cscape parameters during runtime. Such applications are dynamic in that the parameters change when the program is executing. Note that the Cscape configuration is used during power-up and continues until the program overrides the configuration.

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes during runtime.

7.5.2 Overriding Cscape Parameters using a Ladder Code Program

Note: If the user intends to change one or more registers using Cscape Override Procedures, ALL registers must be configured from the ladder code as specified in the Cscape Override section for that option.

A ladder code program must be written to allow the override of the Cscape configuration during runtime. The programmer needs to manually set values into many of the registers that Cscape normally configures. Although the ladder code program is used *during runtime* to override the Cscape setup, the standard Cscape configuration procedures must still be performed in order to download the necessary parameters required by the OCS/RCS for power-up. At runtime, the ladder program assumes control and overrides the Cscape configuration parameters.

The following registers need to be manually set using the ladder code program that is written to override the Cscape configuration.

1. Set %Q7 to 1 in the OCS/RCS to override the Cscape configuration of the input signal condition.

Table 7.4 – OCS/RCS Register

Register	Description
%Q7	Set to 1

To override the Cscape Input Signal Conditioning:

%Q1 and %Q2 control the input threshold, and %Q3 and %Q4 control the noise filter.
%Q5 and %Q6 are optional inputs into the programmed function block.

Table 7.5 – Input Signal Conditioning		
%Q1	%Q2	Input Threshold
0	0	12 VDC for 24 volt systems.
1	0	6 VDC for 12 volt systems
0	1	1.4 VDC for TTL compatibility
1	1	0 VDC for AC coupled signals
%Q3	%Q4	Noise filter / Maximum operating frequency
0	0	High frequency / 1MHz
0	1	Medium frequency / 100KHz
1	X	Low frequency / 10KHz

NOTES

CHAPTER 8: OPTION 6

Diagnostic Tool

8.1 Option 6 Overview

8.1.1 General

Initial configuration procedures to select Option 6 are contained in Chapter Two. The following topics pertaining to Option 6 are covered in Chapter Eight:

a. Function
b. Registers (Checking Direct I/O and System I/O Functions)
c. I/O Map - shows functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.
d. Configuration procedures
e. Advanced Use-Cscape Override Configuration Procedures – used only for applications needing to override the Cscape setup during runtime. Not used in most applications.

8.1.2 Safety Warning

Warning: Failure to disable the High Speed Counter Module (HSC600/601) manually through the ladder code program could cause either personal injury or damage to equipment.

When the OCS/RCS is in the Idle or Stop modes, the HSC600/601 continues normal operation. **The user must physically disable the HSC600/601 through the ladder code program.**

8.2 Function

Option 6 is a convenient troubleshooting tool that is pre-configured for Direct I/O and System I/O functions. Using predefined registers, a programmer can use Option 6 to write a troubleshooting program for a specific installation.

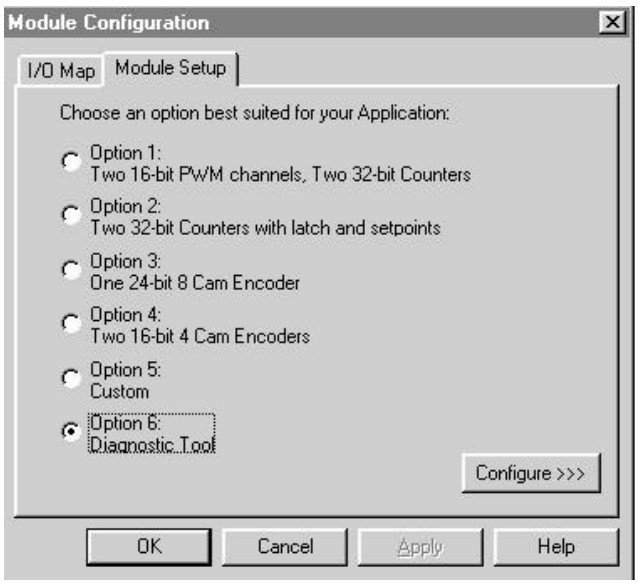


Figure 8.1 – Option 6 Configuration Screen

8.3 Direct I/O Function and Registers

The Direct I/O function allows the user to compare the voltage levels measured at the input and output pins of HSC600/601's connector (J3) to the values in the %I and %Q registers. Eight %I and eight %Q registers are predefined in the OCS/RCS. A read of the %I registers returns the input pins. A write to the %Q registers latches data to the output pins. Refer to Table 8.3 for additional information regarding registers.

Table 8.1 – Direct I/O Registers and Pin-out (J3)

Register	Signal	PIN
%I1	Input1	1
%I2	Input2	2
%I3	Input3	3
%I4	Input4	4
%I5	Input5	5
%I6	Input6	6
%I7	Input7	7
%I8	Input8	8
%Q1	Output1	10
%Q2	Output2	11
%Q3	Output3	12
%Q4	Output4	13
%Q5	Output5	14
%Q6	Output6	15
%Q7	Output7	16
%Q8	Output8	17

8.4 System I/O Function and Registers

The System I/O function checks internal functions of the HSC600/601 as defined in Table 8.2. Eight %I registers, eight %Q registers, and three %AI registers are used for system functions.

The user selects input conditioning parameters (i.e., input voltage threshold and filtering levels) from pull-down menus on the Option 6 screen. If different thresholds and filtering levels are desired *during runtime* than those listed on the Cscape Option 6 screen, the user can modify the Cscape parameters using the Advanced Use –Cscape Override Procedures in Section 8.7. If the override procedures are used, %Q15 (MASK) must be set.

Note: The Cscape Override procedures are <u>not</u> intended for most applications and are recommended only for applications that require parameter changes *during runtime.*

Refer to Table 8.3 for additional information regarding registers.

Table 8.2 – System Registers	
Register	**Description**
%I9	Aux1 read back.
%I10	Aux2 read back
%I11-16	These bits are always zero.
%Q9-10	Voltage Input Select- Normally masked-used during Cscape Override.
%Q11-12	Input Filter Frequency Select-Normally used during Cscape Override.
%Q13	Auxiliary 1
%Q14	Auxiliary 2
%Q15	Leave set to 0 to preserve Cscape setup. This is the MASK (override) bit.
%Q16	Not used.
%AI1 WORD	Option number for configuration verification.
%AI2 WORD	Free-running Counter clocked by 10MHz oscillator.
%AI3 WORD	Free-running Counter clocked by auxiliary oscillator.

8.5 I/O Map

The I/O Map shows the functions that are mapped between the HSC600/601 and the ladder code in the OCS/RCS.

The register blocks that are shown in white are normally accessible using the ladder code. The user sets the parameters. If the user does not set parameters for any one of these blocks, the OCS/RCS automatically writes a zero into the block.

The register blocks that are shown in light gray are automatically configured by Cscape if Q15 (the MASK or override bit) is set to 0. This is the normal setup for most applications. However, in dynamic applications that require parameter changes during runtime, the light gray blocks can be overridden.

Note: The Cscape Override procedures are not intended for most applications and are recommended only for applications that require parameter changes during runtime.

The dark gray blocks are not used.

Table 8.3 – I/O Map										
%I	0	1	2	3	4	5	6	7	8	9
%I 0x		Input1	Input2	Input3	Input4	Input5	Input6	Input7	Input8	Aux1
%I 1x	Aux2									

%Q	0	1	2	3	4	5	6	7	8	9
%Q 0x		Out 1	Out 2	Out 3	Out 4	Out 5	Out 6	Out 7	Out 8	V-in
%Q 1x	V-in	Freq-in	Freq-in	Aux1	Aux2	MASK				

Not used	Masked if MASK (%Q15) is not set.

%AI1	WORD	6 (Option number)
%AI2	WORD	Free-running Counter clocked by 10MHz oscillator.
%AI2	WORD	Free-running Counter clocked by auxiliary oscillator.

Note: This table serves as a general reference for the starting location of the registers. To determine the *actual* starting location of the various registers, it is necessary to consult the "I/O Map" screen in the Cscape Software *after* configuration.

8.6 Configuration Procedures

1. After selecting Option 6 (see Figure 8.1), press **Configure**. The following screen appears.

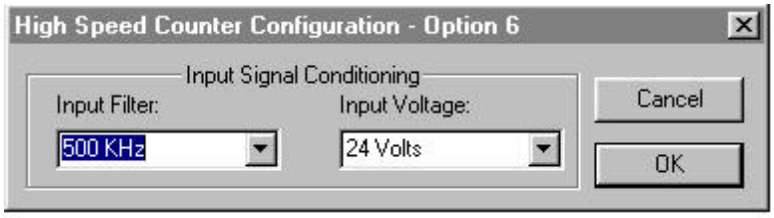


Figure 8.2 – Option 6 Configuration Screen

2. Using pull-down menus, select the input filter value and input voltage value. Press **OK**. When the screen appears, select the **I/O Map** tab, and the following screen appears.

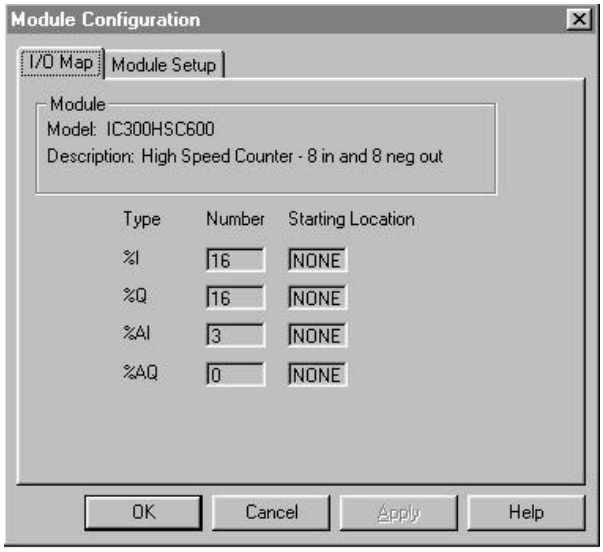


Figure 8.3 – I/O Map Screen

8.7 Advanced Use – Cscape Override Procedures

8.7.1 General

Most application requirements are met using the standard Cscape configuration procedures described earlier in this chapter. The user sets parameters using the Cscape Configuration screen, and the Cscape program has exclusive control over the application at all times. The parameters remain the same (or static) during runtime, and they do not change unless the user reconfigures the setup.

However, there are some applications where it may be necessary to override the Cscape configuration setup *during runtime*. The HSC600/601 gives the user the flexibility of writing a ladder code program to allow changes to the Cscape parameters during runtime. Such applications are dynamic in that the parameters change when the program is executing. Note that the Cscape configuration is used during power-up and continues until the program overrides the configuration.

Note: The Cscape Override procedures are <u>not</u> intended for most applications and are recommended only for applications that require parameter changes during runtime.

8.7.2 Overriding Cscape Parameters using a Ladder Code Program

Note: If the user intends to change one or more registers using Cscape Override Procedures, ALL registers must be configured from the ladder code as specified in the Cscape Override section for that option.

A ladder code program must be written to allow the override of the Cscape configuration during runtime. The programmer needs to manually set values into many of the registers that Cscape normally configures.

Although the ladder code program is used during runtime to override the Cscape setup, the standard Cscape configuration procedures must still be performed in order to download the necessary parameters required by the OCS/RCS for power-up. At runtime, the ladder program assumes control and overrides the Cscape configuration parameters.

The following registers need to be manually set using the ladder code program that is written to override the Cscape configuration.

1. Set %Q15 to 1 to override Cscape's specified parameters for input conditioning (voltage threshold and filtering) and auxiliary levels.

Table 8.4 – OCS/RCS Register	
Register	**Description**
%Q15	Set to 1

To override the Cscape Input Signal Conditioning and Auxiliary Levels:

%Q9 and %Q10 control the input threshold, and %Q11 and %Q12 control the noise filter.
%Q13 is Aux1, and %Q14 is Aux2.

Note: %Q13 and %Q14 are currently not used by this option

Table 8.5 – Input Signal Conditioning Override		
%Q10	**%Q9**	**Input Threshold**
0	0	12 VDC for 24 volt systems.
0	1	6 VDC for 12 volt systems
1	0	1.4 VDC for TTL compatibility
1	1	0 VDC for AC coupled signals
%Q12	**%Q11**	**Noise filter / Maximum Operating Frequency**
0	0	High frequency / 1MHz
0	1	Medium frequency / 100KHz
1	X	Low frequency / 10KHz

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