



*Supplement for
HEC-GV3-DN,
HEC-GV3-RTU*

Reliance GV3000 Drive Registers

PREFACE

This supplement is provided for Horner Electric's HEC-GV3-DN and HEC-GV3-RTU Option Modules for use with Reliance Electric GV3000 AC Drive.

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ABOUT PROGRAMMING EXAMPLES

Any example programs and program segments in this manual or provided on accompanying diskettes are included solely for illustrative purposes. Due to the many variables and requirements associated with any particular installation, Horner Electric cannot assume responsibility or liability for actual use based on the examples and diagrams. It is the sole responsibility of the system designer utilizing HEC-GV3-DN and HEC-GV3-RTU Option Modules to appropriately design the end system, to appropriately integrate the HEC-GV3-DN and HEC-GV3-RTU Option Modules and to make safety provisions for the end equipment as is usual and customary in industrial applications as defined in any codes or standards which apply.

Note: The programming examples shown in this manual are for illustrative purposes only. Proper machine operation is the sole responsibility of the system integrator.

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CHAPTER 1: NETWORK DRIVE REGISTERS

S1.1 Drive Register Table Attributes

Table S.1 includes the following information:

a. Register #:

Indicates the drive register index to be used in the network request.

b. R/W:

Indicates if register is read/write or read only. Attempts to write Read-Only attributes are blocked and generally return a network fault.

c. Access type:

Specifies the register's type for determining access conditions. See "Data Transfer Summary" in the applicable user manual to determine how attribute types affect the acceptance of that register by the drive.

d. Description

Describes the function of the register.

S1.2 Write Access to Drive Registers

Network writes to Drive Data Register require:

1. "Option Card" - Must be selected in the "Control Source Select" (P.000) parameter.
2. If the accessed Register number is greater than 64: "Extended Set" must be selected in the "Network Connection Type (P.061) parameter.
3. If the accessed Register is a Tuneable or Configurable (cfg) type: "Tune/Config Inputs Enable bit" (Reg 32, bit 14) must be set.
4. If the accessed Register is a Configurable (cfg) type: The drive must be stopped.

Table S.1 – Drive Data Registers			
Register#	R/W	Access type	Description
0	RO	Runtime signal	Status word 1 (includes terminal block digital inputs)
			Bit 0 Drive ready
			Bit 1 Drive running
			Bit 2 Fault active
			Bit 3 Jog mode selected
			Bit 4 Reverse commanded
			Bit 5 Stop sequence in-progress
			Bit 6 Tune/Cnfg inputs enabled
			Bit 7 Sync flag echoed from network input
			Bit 8 Terminal block digital input 1 (start)
			Bit 9 Terminal block digital input 2 (stop)
			Bit 10 Terminal block digital input 3 (fault reset)
			Bit 11 Terminal block digital input 4 (run/jog)
			Bit 12 Terminal block digital input 5 (function loss)
			Bit 13 Terminal block digital input 6 (default: Fwd/Rev select) (P.007/P.008)
			Bit 14 Terminal block digital input 7 (default: Ramp1 2 Select) (P.007/P.008)
Bit 15 Terminal block digital input 8 (default: Loc/Rem select) (P.007/P.008)			
1	RO	Runtime signal	Selected speed reference value [4095 = max/top speed] *
2	RO	Runtime signal	Speed sum (sum of ref + draw + trim) [4095 = max/top speed] *
3	RO	Runtime signal	Speed feedback [vector only: 4095 = top speed]
4	RO	Runtime signal	TS analog input [V/H: 10v = 4095 @ max spd, Vector: 10v = 4095 @ top spd] *
5	RO	Runtime signal	RPM display [1=1rpm]
6	RO	Runtime signal	Volts display [1=1volt]
7	RO	Runtime signal	Amps display [1=0.1 amps]
8	RO	Runtime signal	Network Output Register 1 ¹
9	RO	Runtime signal	Network Output Register 2 ²
10	RO	Runtime signal	Network Output Register 3 ³
11	RO	Runtime signal	Network Output Register 4 ⁴
12	RO	Tune/cfg/stat	Fault latch bits, word 1
			Bit 0 Overcurrent steady state
			Bit 1 Overcurrent while accelerating
			Bit 2 Overcurrent while decelerating
			Bit 3 Overcurrent during DC-Braking
			Bit 4 DC bus to high
			Bit 5 DC bus to low
			Bit 6 Electronic thermal overload
			Bit 7 Thermostat over temperature
			Bit 8 Function loss
			Bit 9 EPROM defaults restored
			Bit 10 Loss of comm from serial port
			Bit 11 Spurious UART interrupt
Bit 12 Torque/current Self-tuning fault			

Register #	R/W	Access type	Description
13	RO	Tune/cfg/stat	Bit 13 Overspeed (10% over max speed)
			Bit 14 Output phase loss
			Bit 15 Over frequency
			Fault latch bits word 2
			Bit 0 Network Communications Loss
			Bit1 Bypass contact failure
			Bit2 High-time Identification aborted
			Bit3 Drive not identified
			Bit4 High line voltage
			Bit5 Write to EPROM failure
			Bit6 Power unit overload
			Bit7 Earth current failure
			Bit8 Asymmetrical bus charge
			Bit9 Missing power unit ID connector
			Bit10 Unselected power unit
			Bit11 Input phase loss
Bit12 Encoder loss			
Bit13 Analog input loss (4-20mA < 1mA) ⁵			
Bit14 <unused>			
Bit15 Fatal system error			
14	RO	Tune/cfg/stat	Bit 0-7, Number of error log entries
			Bit 8, one or more parameter processing error flag
			Bit 9-15, <unused>
15	RO	Tune/cfg/stat	Error log entry (n-1)
			Error log entry (n) = most recent
16	RO	Tune/cfg/stat	Active control source: (P.000)
17	RO	Tune/cfg/stat	Accel time (1 = 0.1 sec) (P.001)
18	RO	Tune/cfg/stat	Decel time (1 = 0.1 sec) (P.002)
19	RO	Tune/cfg/stat	Minimum speed (V/H: 1 = 0.1 hz, Vector: 1 = 1 RPM) (P.003)
20	RO	Tune/cfg/stat	Maximum speed (V/H: 1 = 0.1 hz, Vector: 1 = 1 RPM) (P.004)
21	RO	Tune/cfg/stat	Current limit (1 = 1% motor nameplate amps) (P.005)
22	RO	Tune/cfg/stat	Trim gain (1 = 0.001) (P.015)
23	RO	Tune/cfg/stat	Draw gain (1 = 0.001) (P.016)
24	RO	Tune/cfg/stat	(Vector) Speed proportional gain (1 = 0.01) (U.012)
25	RO	Tune/cfg/stat	(Vector) Speed integral gain (1 = 0.01) (U.013)
26	RO	Tune/cfg/stat	Status Word 2
			Bit0 Vector speed/trq regulation (0=torque, 1=speed)
			Bit1 Manual reference selected (0=auto ref, 1=manual ref (FP setpoint))
			Bit2 Outer control loop (OCL) enabled (0=disabled, 1 = enabled) ⁵
			Bit3-15 <Unused>
27	RO	Tune/cfg/stat	Elapsed time meter readout (1 = 1day) (P.029)

Register#	R/W	Access type	Description
28	RO	Tune/cfg/stat	Network Connection type (P.061)
29	RO	Tune/cfg/stat	Option communications loss response (P.062)
30	RO	Tune/cfg/stat	Bit0-7 Network Configuration (P.063)
			Bit8-15 Network trim reference source (P.064) ⁵
31	RO	Tune/cfg/stat	Drive software version (P.098)
32	R/W	Control/ref	Drive control word
			Bit 0 start
			Run mode (^ to start)
			Jog mode (1 = start, 0 = stop)
			Bit 1 stop (0 = stop, 1 = not stop)
			Bit 2 fault reset (^ to reset)
			Bit 3 run/jog select (0 = run, 1 = jog)
			Bit 4 fwd/rev select (0=fwd, 1=rev)
			Bit 5 outer control loop (OCL) enable ⁵
			Bit 6 <reserved> must be zero
			Bit 7 speed/trq reg select (0=trq based on U.000, 1=speed, regardless of U.000)
			Bit 8 error log clear command
			Bit9-13 <reserved> must be zero
			Bit 14 tune/cnfg input enable command
			(0 = update control/ref data only from network)
			(1 = update all inputs from network)
			Bit 15 sync flag echoed to network output
33	R/W	Control/ref	Network speed/torque reference (4095 = max/top speed) *
34	R/W	Control/ref	Network trim reference (used when P.014 = 2, 4095 = max/top speed) *
35	R/W	Control/ref	Network Inertia compensation ⁵
36			<reserved> must be zero
37	R/W	Tunable	Accel time (1 = 0.1 sec) (P.001)
38	R/W	Tunable	Decel time (1 = 0.1 sec) (P.002)
39	R/W	Tunable	Minimum speed (V/H: 1 = 0.1 hz, Vector: 1 = 1 RPM) (P.003)
40	R/W	Tunable	Maximum speed (V/H: 1 = 0.1 hz, Vector: 1 = 1 RPM) (P.004)
41	R/W	Tunable	Current limit (1 = 1% motor nameplate amps) (P.005)
42	R/W	Tunable	TS analog input offset (P.009)
43	R/W	Tunable	TS analog input gain (1 = 0.001) (P.010)
44	R/W	Tunable	TS analog input configure (P.011) ⁵
45	R/W	Tunable	Trim gain (1 = 0.001) (P.015)
46	R/W	Tunable	Draw gain (1 = 0.001) (P.016)
47	R/W	Tunable	(Vector) Speed proportional gain (1 = 0.01) (U.012)
48	R/W	Tunable	(Vector) Speed integral gain (1 = 0.01) (U.013)
49	R/W	Tunable	Jog reference (V/H: 1 = 0.1Hz, Vector:: 1 = 1 RPM) (P.020)

Register#	R/W	Access type	Description
50	R/W	Tunable	Stop configuration (0 = coast, 1 = ramp) (P.025)
51	R/W	Tunable	Function loss response (P.026)
52	R/W	Tunable	RPM display scale (P.028)
53	WO	Tunable	Control Booleans
			Bit0 Elapsed time meter reset (on 0 to 1 transition) (P.030)
			Bit1 Network inertia comp reg enable (enables use of drop 1, reg 35) ⁵
			Bit2 Network speed PI limi control enable (enables drop 1, reg 59 and 60) ⁵
			Bit3-15 <reserved> must be zero
54			<reserved> must be zero
55			<reserved> must be zero
56	R/W	Configurable	Output relay configuration (P.013)
57	R/W	Configurable	Trim reference source (P.014)
58	R/W	Configurable	Bit0-7 Torque reference source (U.000)
			Bit8-15 OCL feedback source (U.040) ⁵
59	R/W	Configurable	Network speed PI high limit ⁵
60	R/W	Configurable	Network speed PI low limit ⁵
61	R/W	Configurable	Option Network connection type (0=partial, 1=full) (P.061)
62	R/W	Tunable	Option communications loss selection (P.062)
63	R/W	Configurable	Bit0-7 Network Configuration (P.063)
			Bit8-15 Option time ref select (P.064) ⁵

IMPORTANT: The remaining data is only accessible if Register #61 (Network connection type) is set to 1, full network connection. Note that if the full network connection is selected, the drive will read ALL of the output data, therefore if any of the following outputs are to be controlled by the network master, ALL of them must be controlled by the network master.

Register #	R/W	Access type	Description
64	RO		Torque reference
65	RO		Torque feedback
66	RO		<Unused>
67	RO		Bit0-7 Network Output register 1 select ⁵
			Bit8-15 Network Output register 2 select ⁵
68	RO		Bit0-7 Network Output register 3 select ⁵
			Bit8-15 Network Output register 4 select ⁵
69	RO	Tune/cfg/stat	TS analog input offset (P.009)
70	RO	Tune/cfg/stat	TS analog input gain (P.010)
71	RO	Tune/cfg/stat	TS analog input cnf (P.011) ⁵
72	RO	Tune/cfg/stat	TS analog output select (P.012)
73	RO	Tune/cfg/stat	Ts relay configure (P.013)
74	RO	Tune/cfg/stat	Trim reference source select (P.014)
75	RO	Tune/cfg/stat	S-curve enable (P.019)
76	RO	Tune/cfg/stat	Jog reference (P.020)
77	RO	Tune/cfg/stat	Jog accel time (1 = 0.1) (P.021)
78	RO	Tune/cfg/stat	Jog decel time (1 = 0.1) (P.022)
79	RO	Tune/cfg/stat	Bit0-7 Stop type (P.025)

Register #	R/W	Access Type	Description
			Bit8-15 <Unused>
80	RO	Tune/cfg/stat	Function loss response (P.026)
81	RO	Tune/cfg/stat	Fwd/Rev configuration (P.027)
82	RO	Tune/cfg/stat	RPM display scale (P.028)
83	RO	Tune/cfg/stat	Configuration Booleans
			Bit0 Electronic thermal overload enable (P.040)
			Bit1 Level sense start enable (P.054) ⁵
			Bit2 Low bus fault avoidance enable (SVC only) (U.023) ⁵
			Bit3 High bus fault avoidance enable (FVC & SVC only) (U.024) ⁵
			Bit4 OCL proportional trim enable (U.048) ⁵
			Bit5-15 <Unused>
84	RO	Tune/cfg/stat	Electronic thermal overload type (P.041)
85	RO	Tune/cfg/stat	(V/H) Line dip time (P.042)
86	RO	Tune/cfg/stat	Auto reset attempts (P.043)
87	RO	Tune/cfg/stat	Auto reset time (P.044)
88	RO	Tune/cfg/stat	Tunable Booleans
			Bit0 Encoder loss enable (P.039)
			Bit1 Output Phase loss enable (P.045)
			Bit2 Manual ref preset enable (P.053)
			Bit3 Auto/Man key disable (P.052) ⁵
			Bit4 Stop key disable (P.055) ⁵
			Bit5-15 <Unused>
89	RO	Tune/cfg/stat	Current compounding gain (U.026) ⁵
90	RO	Tune/cfg/stat	Carrier frequency select (0 = 2 KHz, 1 = 4 KHz, 2 = 8 KHz) (P.047)
91	RO	Tune/cfg/stat	Control type (0=V/H, 1=Vector) (P.048)
92	RO	Tune/cfg/stat	Default type (P.049)
93	RO	Tune/cfg/stat	Inertia compensation gain (U.027) ⁵
94	RO	Tune/cfg/stat	Losses gain (U.028) ⁵
95	RO	Tune/cfg/stat	Option type and version number (P.065)
96			<reserved> must be zero
97			<reserved> must be zero
98	R/W	Tunable	Bit0-7 TS analog output select (P.012)
			Bit8-15 <reserved> must be zero
99	R/W	Tunable	Jog accel time (1 = 0.1 sec) (P.021)
100	R/W	Tunable	Jog decel time (1 = 0.1 sec) (P.022)
101	R/W	Tunable	Fwd/Rev configure (P.027)
102	R/W	Tunable	Tunable Booleans
			Bit0 Encoder loss enable (P.039)
			Bit1 Output phase loss enable (P.045)
			Bit2 Manual ref preset enable (P.053)
			Bit3 Auto/Man key disable (P.052) ⁵
			Bit4 Stop key disable (P.055) ⁵
			Bit5-15 <reserved> must be zero
103	R/W	Configurable	S-curve enable (P.019)
104	R/W	Configurable	Configurable Booleans
			Bit0 Electronic thermal overload enable (P.040)

Register #	R/W	Access Type	Description
104 cont.	R/W	Configurable	Bit1 Level sense start enable (P.054) ⁵
			Bit2 Low bus fault avoidance enable (SVC only) (U.023) ⁵
			Bit3 High bus fault avoidance enable (FVC & SVC only) (U.024) ⁵
			Bit4 OCL proportional trim enable (U.048) ⁵
			Bit5-15 <reserved> must be zero
105	R/W	Configurable	Electronic thermal overload type (P.041)
106	R/W	Configurable	(V/H) Line dip ride-through time (P.042)
107	R/W	Configurable	Auto reset attempts (P.043)
108	R/W	Configurable	Auto reset time (P.044)
109	R/W	Tunable	Bit0-7 Network output reg 1 select (P.066) ⁵
			Bit8-15 Network output reg 2 select (P.067) ⁵
110	R/W	Tunable	Bit0-7 Network output reg 3 select (P.068) ⁵
			Bit8-15 Network output reg 4 select (P.069) ⁵
111	R/W	Configurable	Carrier frequency select (0 = 2 KHz, 1 = 4 KHz, 2 = 8 KHz) (P.047)
112			<reserved> must be zero
113	R/W	Configurable	Default type (0 = USA, 1 = EUr, 2 = JPN) (P.049)
114-127			<reserved> must be zero
128	RO	Tune/cfg/stat	(Vector) Bit0-7 Torque reference select (U.000)
			(Vector) Bit8-15 OCL feedback source (U.040) ⁵
			(V/H) Motor nameplate volts (H.000)
129	RO	Tune/cfg/stat	(Vector) pulse encoder PPR select (0 = 512, 1 = 1024, 2 = 2048, 3 = 4096, 4 = SE) (U.001)
			(V/H) Motor nameplate base frequency (1 = 0.1 hz) (H.001)
130	RO	Tune/cfg/stat	(Vector) Motor pole number select (0=2, 1=4, 2=6, 3=8 poles) (U.002)
			(V/H) Motor nameplate amps (1 = 0.1 amps) (H.002)
131	RO	Tune/cfg/stat	(Vector) Motor base frequency (1 = 0.1 hz) (U.003)
			(V/H) Torque boost voltage (1 = 0.1% of nominal inverter voltage) (H.003)
132	RO	Tune/cfg/stat	(Vector) Motor rated amps (1 = 0.1 amps) (U.004)
			(V/H) Slip compensation (1 = 0.01% of base frequency) (H.004)
133	RO	Tune/cfg/stat	(Vector) Motor rated RPM (U.005)
			(V/H) DC braking enable (H.005)
134	RO	Tune/cfg/stat	(Vector) Motor magnetizing amps percent (magnetizing amps / rated amps * 1000) (U.006)
			(V/H) DC braking start frequency (1 = 0.1 hz) (H.006)
135	RO	Tune/cfg/stat	(Vector) Motor rated volts (U.007)
			(V/H) DC braking current (1 = 1.0% of rated motor amps) (H.007) ⁶
136	RO	Tune/cfg/stat	(Vector) speed loop self-tuning result (U.009)
			(V/H) DC braking time (1 = 0.1 sec) (H.008)
137	RO	Tune/cfg/stat	(Vector) <Unused>
			(V/H) Avoidance frequency enable (H.009)

Register #	R/W	Access Type	Description
138	RO	Tune/cfg/stat	(Vector) Torque proportional gain (* 100) (U.014)
			(V/H) Avoidance frequency midpoint 1 (1 = 0.1 hz) (H.010)
139	RO	Tune/cfg/stat	(Vector) Torque integral gain (* 10) (U.015)
			(V/H) Avoidance frequency band 1 (1 = 0.1 hz) (H.011)
140	RO	Tune/cfg/stat	(Vector) Field weakening start RPM (U.016)
			(V/H) Avoidance frequency midpoint 2 (1 = 0.1 hz) (H.012)
141	RO	Tune/cfg/stat	(Vector) Top speed (RPM) (U.017)
			(V/H) Avoidance frequency band 2 (1 = 0.1 hz) (H.013)
142	RO	Tune/cfg/stat	(Vector) AC line volts (U.018)
			(V/H) Avoidance frequency midpoint 3 (1 = 0.1 hz) (H.014)
143	RO	Tune/cfg/stat	(Vector) Flux loop proportional gain (1 = 0.01) (U.019)
			(V/H) Avoidance frequency band 3 (1 = 0.1 hz) (H.015)
144	RO	Tune/cfg/stat	(Vector) Flux loop integral gain (1 = 0.1 hz) (U.020)
			(V/H) Sync direction (H.016)
145	RO	Tune/cfg/stat	(Vector) Rotor time constant (1 = 0.001 sec) (U.021)
			(V/H) Input power/snubber configuration (H.017)
146	RO	Tune/cfg/stat	(Vector) Motor rated HP (1 = 0.1 HP) (U.022) ⁵
			(V/H) V/Hz curve (H.018)
147	RO	Tune/cfg/stat	(Vector) Zero speed hold time (1 = 0.1 sec) (U.025) ⁵
			(V/H) Identification results (H.019)
148	RO	Tune/cfg/stat	(Vector) SVC slip adjust (1 = 0.01) (U.030) ⁵
149	RO	Tune/cfg/stat	(Vector) Bit0-7 SVC sync select (U.031) ⁵
			(Vector) Bit8-15 OCL L/L select (0 = bypass, 1 = lead/lag, 2 = lag/lead) (U.041) ⁵
			(V/H) AC Line volts (H.021)
150	RO	Tune/cfg/stat	(Vector) SVC flux current reg gain (U.032) ⁵
			(V/H) Overfrequency limit (1 = 0.1 hz) (H.022)
151	RO	Tune/cfg/stat	(Vector) OCL L/L low frequency (1 = 0.01 rad/sec) (U.042) ⁵
152	RO	Tune/cfg/stat	(Vector) OCL L/L ratio (1 = 1) (U.043) ⁵
153	RO	Tune/cfg/stat	(Vector) OCL reference gain (1 = 0.001) (U.044) ⁵
154	RO	Tune/cfg/stat	(Vector) OCL proportional gain (1 = 0.01) (U.045) ⁵
155	RO	Tune/cfg/stat	(Vector) OCL integral gain (1 = 0.01) (U.046) ⁵
			(V/H) Power module output amps (P.095)
156	RO	Tune/cfg/stat	Panel amps (1 = 0.1 amps) (F.000)
157	RO	Tune/cfg/stat	Panel volts (1 = 1 volt) (F.001)
158	RO	Tune/cfg/stat	(Vector) OCL trim range (1 = 0.001) (U.047) ⁵
			(V/H) <reserved> must be zero
159	RO	Tune/cfg/stat	Power module type (P.099)
160	R/W	Configurable	(Vector) Pulse encoder PPR select (0 = 512, 1 = 1024, 2 = 2048, 3 = 4095, 4 = SE) (U.001)
			(V/H) Motor nameplate volts (H.000)
161	R/W	Configurable	(Vector) Motor pole number select (0=2, 1=4, 2=6, 3=8) (U.002)
			(V/H) Motor nameplate base frequency (1 = 0.1 hz) (H.001)
162	R/W	Configurable	(Vector) Motor base frequency (1 = 0.1 hz) (U.003)
			(V/H) Motor nameplate amps (1 = 0.1 amps) (H.002)

Register #	R/W	Access Type	Description
163	R/W	Configurable	(Vector) Motor rated amps (1 = 0.1 amps) (U.004)
			(V/H) Torque boost voltage (1 = 0.1% of nominal inverter voltage) (H.003)
164	R/W	Configurable	(Vector) Motor rated RPM (U.005)
			(V/H) Slip compensation(1 = 0.01% of base frequency) (H.004)
165	R/W	Configurable Tunable	(Vector) Motor magnetizing amps percent (magnetizing amps / rated amps * 1000) (U.006)
			(V/H) DC braking enable (H.005)
166	R/W	Configurable Tunable	(Vector) Motor rated volts (U.007)
			(V/H) DC braking start frequency (1 = 0.1 hz) (H.006)
167	R/W	Tunable	(Vector) Torque proportional gain (* 100) (U.014)
			(V/H) DC braking current (1 = 1.0% of rated motor amps) (H.007) ⁶
168	R/W	Tunable	(Vector) Torque integral gain (* 10) (U.015)
			(V/H) DC braking time (1 = 0.1 sec) (H.008)
169	R/W	Configurable Tunable	(Vector) Field weakening start RPM (U.016)
			(V/H) Avoidance frequency enable (H.009)
170	R/W	Configurable Tunable	(Vector) Top speed (RPM) (U.017)
			(V/H) Avoidance frequency midpoint 1(1 = 0.1 hz) (H.010)
171	R/W	Configurable Tunable	(Vector) AC line volts (U.018)
			(V/H) Avoidance frequency band 1 (1 = 0.1 hz) (H.011)
172	R/W	Tunable	(Vector) Flux loop proportional gain (1 = 0.01) (U.019)
			(V/H) Avoidance frequency midpoint 2 (1 = 0.1 hz) (H.012)
173	R/W	Tunable	(Vector) Flux loop integral gain (1 = 0.1) (U.020)
			(V/H) Avoidance frequency band 2 (1 = 0.1 hz) (H.013)
174	R/W	Tunable	(Vector) Rotor time constant (1 = 0.001 sec) (U.021)
			(V/H) Avoidance frequency midpoint 3 (1 = 0.1 hz) (H.014)
175	R/W	Configurable Tunable	(Vector) Motor rated HP (1 = 0.1 HP) (U.022) ⁵
			(V/H) Avoidance frequency band 3 (1 = 0.1 hz) (H.015)
176	R/W	Tunable Configurable	(Vector) Zero speed hold time (1 = 0.1 sec) (U.025) ⁵
			(V/H) Sync direction (H.016)
177	R/W	Tunable Configurable	(Vector) Current compounding gain (U.026) ⁵
			(V/H) Input power/snubber configuration (H.017)
178	R/W	Tunable Configurable	(Vector) Inertia compounding gain (U.027) ⁵
			(V/H) V/Hz curve select (H.018)
179	R/W	Tunable	(Vector) Losses gain (U.028) ⁵
			(V/H) <reserved> must be zero
180			<reserved> must be zero
181	R/W	Tunable Configurable	(Vector) SVC slip adjust (1 = 0.1) (U.030) ⁵
			(V/H) AC Line volts (H.021)

Register #	R/W	Access Type	Description
182	R/W	Configurable	(Vector) Bit0-7 SVC sync select (U.031) ⁵
		Tunable	(Vector) Bit8-15 OCL L/L select (0=bypass, 1=lead/lag, 2=l原因/lead) (U.041) ⁵
		Configurable	(V/H) Overfrequency limit (1 = 0.1 hz) (H.022)
183	RW	Tune/cfg/stat	(Vector) SVC flux current reg gain (1 = 1 rad/sec) (U.032) ⁵
			(V/H) <reserved> must be zero
184			<reserved> must be zero
185	RW	Tunable	(Vector) OCL L/L low frequency (1 = 0.01 rad/sec) (U.042) ⁵
			(V/H) <reserved> must be zero
186	RW	Tunable	(Vector) OCL L/L ratio (1 = 1) (U.043) ⁵
			(V/H) <reserved> must be zero
187	RW	Tunable	(Vector) OCL reference gain (1 = 0.001) (U.044) ⁵
			(V/H) <reserved> must be zero
188	RW	Tunable	(Vector) OCL proportional gain (1 = 0.01) (U.045) ⁵
			(V/H) <reserved> must be zero
189	RW	Tunable	(Vector) OCL integral gain (1 = 0.01) (U.046) ⁵
			(V/H) <reserved> must be zero
190	RW	Tunable	(Vector) OCL trim range (1 = 0.001) (U.047) ⁵
			(V/H) <reserved> must be zero
191			<reserved> must be zero
* Max speed corresponds to P.004 in V/H mode Top speed corresponds to U.017 in Vector mode			
¹ Output Power prior to Controller Firmware Ver. 6.0.			
² Output Torque prior to Controller Firmware Ver. 6.0			
³ Output Power Factor prior to Controller Firmware Ver. 6.0.			
⁴ Pulsetach Counter prior to Controller Firmware Ver. 6.0.			
⁵ Added Parameter to Controller Firmware Ver. 6.0.			
⁶ Parameter changed from voltage to current with Controller Firmware Ver. 6.0			