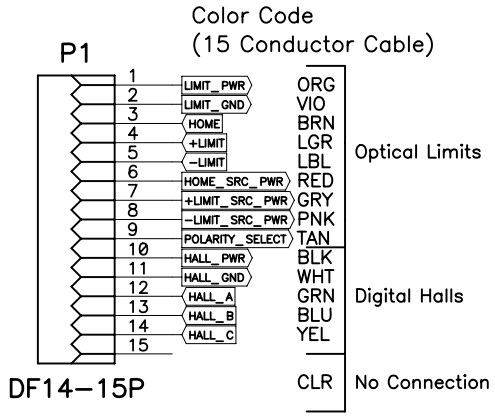
Digital Hall Notes:

The digital hall effect circuit is electrically isolated from the optical limit circuit.
+5 to +15 Vdc is required from HALL_PWR (P1–10) to HALL_GND (P1–11) to power the hall effects.
The hall effect outputs are NPN open collector (sinking) rated at 10 mA, 15 V max.
The hall effect phasing and color code is specified in the Trilogy standard forward timing diagram.

Optical Limit Notes:

The optical limit circuit is electrically isolated from the digital hall circuit.
+5 to +24 Vdc is required from LIMIT_PWR (P1–1) to LIMIT_GND (P1–2).



The limit outputs are full drivers. They can both sink (NPN) and source (PNP) current.
Each limit output has a corresponding source power pin. Each output will be pulled to the voltage level on its source power pin when sourcing.
If sourcing is not required the source power pin for any limit output may be left unconnected.
If a source power pin is left unconnected then its corresponding limit output will be only a sinking (NPN open collector type) output.
The source power pins can be connected to any voltage up to +24 Vdc. The voltages powering the limits and each of the source power pins are completely independent and may be any combination up to their rated limits.

Each limit output is rated at 24 Vdc and 25 mA (sink or source) MAX.

DEFAULT LIMIT OUTPUT POLARITY:
The limit outputs are pulled low (to LIMIT_GND) when the sensor IS NOT on a reflective surface.
The limit outputs are pulled high (to their source power pin) when the sensor IS on a reflective surface (if the source power pin IS connected).
The limit outputs are floating (open collector) when the sensor IS on a reflective surface (if the source power pin IS NOT connected).

ALTERNATE LIMIT OUTPUT POLARITY:
The limit output polarity for all limits can be inverted by connecting POLARITY_SELECT (P1–9) to LIMIT_GND (P1–2).
Inverting the limit output polarity will make the outputs behave as described above in the "Default Limit Output Polarity" section except that reflective and non–reflective surfaces will be exchanged. If the alternate polarity is NOT desired, do NOT connect POLARITY_SELECT to anything. Leave it floating. Make sure it does not short the the shield.

Connector Notes:

Mating connector for P1 is
Hirose Electric part # DF14–15S–1.25C (DigiKey # H1572).

Tin crimp terminals for 26–28 AWG wire is
Hirose Electric part # DF14–2628SCF (DigiKey # H1576CT).

Title	Optical DHED/Limit Head Board Part # HED–1, HED–4	
Size: A	Number: I/O Pinout and Notes	Rev: C
Date: 3–11–05		Drawn by: David Hoffman
Filename: HED–1–4 Rev C.sch		Sheet 4 of 4

Digital Hall Notes:

The digital hall effect circuit is electrically isolated from the optical limit circuit.
+5 to +24 Vdc is required from HALL_PWR (P1–10) to HALL_GND (P1–11) to power the hall effects.
The hall effect outputs are NPN open collector (sinking) rated at 20 mA, 24 V max.
The hall effect phasing and color code is specified in the Trilogy standard forward timing diagram.

Magnetic Limits Notes:

The limit circuit is electrically isolated from the digital hall circuit.
+5 to +24 Vdc is required from LIMIT_PWR (P1–1) to LIMIT_GND (P1–2).

The limit outputs are full drivers. They can both sink (NPN) and source (PNP) current.
Each limit output has a corresponding source power pin. Each output will be pulled to the voltage level on its source power pin when sourcing.
If sourcing is not required the source power pin for any limit output may be left unconnected.
If a source power pin is left unconnected then its corresponding limit output will only be a sinking (NPN type) output.
The source power pins can be connected to any voltage up to +24 Vdc. The voltages powering the limits and each of the source power pins are completely independent and may be any combination up to their rated limits.

Each limit output is rated at 24 Vdc and 25 mA (sink or source) MAX.

DEFAULT LIMIT OUTPUT POLARITY:
The limit outputs are pulled low (to LIMIT_GND) when the sensor IS NOT on a limit magnet.
The limit outputs are pulled high (to their source power pin) when the sensor IS on a limit magnet (if the source power pin IS connected).
The limit outputs are floating (open collector) when the sensor IS on a limit magnet (if the source power pin IS NOT connected).

ALTERNATE LIMIT OUTPUT POLARITY:
The limit output polarity for all limits can be inverted by connecting POLARITY_SELECT (P1–9) to LIMIT_GND (P1–2).
Inverting the limit output polarity will make the outputs behave as described above in the "Default Limit Output Polarity" section except that regions with limit magnets and regions without limit magnets will be exchanged. If the alternate polarity is NOT desired, do NOT connect POLARITY_SELECT to anything. Leave it floating. Make sure it does not short the the shield.

Color Code
(15 Conductor Cable)

P1

1	LIMIT_PWR	ORG	
2	LIMIT_GND	VIO	
3	HOME	BRN	
4	+LIMIT	LGR	Magnetic Limits
5	–LIMIT	LBL	
6	HOME_SRC_PWR	RED	
7	+LIMIT_SRC_PWR	GRY	
8	–LIMIT_SRC_PWR	PNK	
9	POLARITY_SELECT	TAN	
10	HALL_PWR	BLK	
11	HALL_GND	WHT	
12	HALL_A	GRN	Digital Halls
13	HALL_B	BLU	
14	HALL_C	YEL	
		CLR	No Connection

RoHS Compliance Notes:

The PCB and all electronic components are ~~RoHS compliant as of Revision C.~~

Connector Notes:

Mating connector for P1 is
Hirose Electric part # DF11–14DS–2C (DigiKey # H2140).

Tin crimp terminals for 24–28 AWG wire is
Hirose Electric part # DF11–2428SC ~~(DigiKey # H2139).~~

Title	~~HED–10–xx HED–60–xx~~ Limit/DHED Board		
Size: A	Number: I/O Pinout	Rev: D	
Date: ~~3–20–06~~		Drawn by: David Hoffman	
Filename: ~~HED–10–60 Rev D.sch~~		Sheet 3 of 4	