The following is an example of the necessary query and corresponding response for holding register 2 . In this example register 2 is the decimal value 123 Query: 010300010001 D5 CA Response: 01030200 7B F8 67
Notes:

1. The PAX2C registers can be read as holding ( 4 x ) or input ( 3 x ) registers.
2. The PAX2C should not be powered down while parameters are being changed. Doing so may corrupt the non-volatile memory resulting in checksum errors.

## PAX2C Ver 2.0 Modbus Register Table

| REGISTER <br> ADDRESS | REGISTER NAME | LOW <br> LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FREQUENTLY USED REGISTERS |  |  |  |  |  |  |
| 01 | Input Process Value | N/A | N/A | N/A | Read | 1 = 1 Display Unit |
| 02 | Maximum Value | -1999 | 9999 | N/A | Read | 1 = 1 Display Unit |
| 03 | Minimum Value | -1999 | 9999 | N/A | Read | 1 = 1 Display Unit |
| 04 | Active Setpoint Value | SPLO | SPHI | 0 | Read/Write | 1 = 1 Display Unit; Limited by setpoint low/high limits |
| 05 | Setpoint 1 Value | SPLO | SPHI | 0 | Read/Write | 1 = 1 Display Unit; Limited by setpoint low/high limits |
| 06 | Setpoint 2 Value | SPLO | SPHI | 0 | Read/Write | 1 = 1 Display Unit; Limited by setpoint low/high limits |
| 07 | Setpoint Deviation | N/A | N/A | N/A | Read Only | 1 = 1 Display Unit |
| 08 | Output Power | -1000 | 1000 | N/A | Read/Write | Output Power: Heat/Cool; * writable only in manual mode; $1=0.1 \%$ |
| 09 | Active Proportional Band | 0 | 9999 | 700 | Read/Write | 1 = 1 Display Unit |
| 10 | Active Integral Time | 0 | 65000 | 120 | Read/Write | 1 = 0.1 Second |
| 11 | Active Derivative Time | 0 | 9999 | 30 | Read/Write | 1 = 0.1 Second |
| 12 | Active Power Filter | 0 | 600 | 10 | Read/Write | 1 = 0.1 Second |
| 13 | Auto-Tune Code | 0 | 4 | 2 | Read/Write | 0 = Very Aggressive, 1 = Aggressive, 2 = Default, 3 = Conservative, 4 = Very Conservative |
| 14 | Auto-Tune Request | 0 | 1 | 0 | Read/Write | ```0 = Off, 1 = Invoke Auto-Tune , 2 = Auto-Tune CS1, 3 = Auto-Tune CS2, 4 = Auto-Tune CS3, 5 = Auto-Tune CS4, 6 = Auto-Tune CS5, 7 = Auto-Tune CS6``` |
| 15 | Auto-Tune Phase | 0 | 4 | 0 | Read | 0 = Off, 4 = Last Phase of Auto-Tune |
| 16 | Auto-Tune Done | 0 | 1 | 0 | Read | 1 = Successful Auto-Tune since last power cycle. |
| 17 | Auto-Tune Fail | 0 | 1 | 0 | Read | 0 = Off, 1 = Auto-Tune failed |
| 18 | Control Mode | 0 | 1 | 0 | Read/Write | 0 = Automatic, 1 = Manual Mode |
| 19 | Setpoint Selection | 0 | 1 | 0 | Read/Write | 0 = Setpoint 1, 1 = Setpoint $2 \ldots 5$ = Setpoint 6 |
| 20 | Remote/Local Setpoint Selection | 0 | 1 | 0 | Read/Write | 0 = Local, 1 = Remote |
| 21 | PID Set Selection | 0 | 1 | 0 | Read/Write | 0 = PID Set 1 (Pri), 1 = PID Set 2(Alt), 2 = PID Set 3, 3 = PID Set 4, 4 = PID Set 5, $5=$ PID Set $6,6=$ SPSL, $7=$ Auto |
| 22 | Disable Integral Action | 0 | 1 | 0 | Read/Write | 0 = Enabled, 1 = Disabled |
| 23 | Disable Setpoint Ramping | 0 | 1 | 0 | Read/Write | 0 = Enabled, 1 = Disabled |
| 24 | Setpoint Ramping In Process | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = In Process |
| 25 | Setpoint Ramp Rate Value | -1999 | 9999 | 0 | Read/Write | 1 = 0.1 Setpoint Ramping @ Timebase unit selection |
| 26 | Alarm (1-16) Status Register | 0 | 65535 | 3 | Read | Bit 15 = A16, Bit $0=$ A1 |
| 27 | PID Stop/Run | 0 | 1 | 0 | Read/Write | 0 = Run PID, 1 = Stop PID (Output Power = 0\%) |
| 28 | User Input Status | 0 | 2 | 0 | Read | Bit 1 = User Input 2, Bit 0 = User Input 1 |
| 29 | Digital Output Status | 0 | 15 | N/A | Read/Write | Status of Digital Outputs. Bit State: $0=$ Off, $1=$ On. <br> Bit 3 = Out1, Bit $2=$ Out2, Bit $1=$ Out3, Bit $0=$ Out4. <br> Outputs can only be activated/reset with this register when the respective bits in the Manual Mode Register (MMR) are set. |
| 30 | Output Manual Mode Register (MMR) | 0 | 31 | 0 | Read/Write | Bit State: $0=$ Auto Mode, 1 = Manual Mode <br> Bit $4=\mathrm{DO} 1$, Bit $3=\mathrm{DO} 2$, Bit $2=\mathrm{DO} 3$, Bit $1=\mathrm{DO} 4$, Bit $0=$ Linear Output |
| 31 | Alarm Reset Register | 0 | 65535 | 0 | Read/Write | Bit State: 1 = Reset Alarm, bit is returned to zero following reset processing; Bit $15=\mathrm{A} 16$, Bit $0=\mathrm{A} 1$ |


| REGISTER ADDRESS | REGISTER NAME | LOW LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 32 | Analog Output Register (AOR) | 0 | 4095 | 0 | Read/Write | Functional only if Linear Output is in Manual Mode.(MMR bit $0=1$ ) Linear Output Card written to only if Linear Out (MMR bit 0) is set. |
| 33 | Active Alarm 1 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 34 | Active Alarm 2 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 35 | Active Alarm 3 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 36 | Active Alarm 4 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 37 | Active Alarm 5 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 38 | Active Alarm 6 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 39 | Active Alarm 7 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 40 | Active Alarm 8 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 41 | Active Alarm 9 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 42 | Active Alarm 10 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 43 | Active Alarm 11 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 44 | Active Alarm 12 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 45 | Active Alarm 13 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 46 | Active Alarm 14 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 47 | Active Alarm 15 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 48 | Active Alarm 16 Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B); 1 = 1 Display Unit |
| 49 | Active Alarm 1 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 50 | Active Alarm 2 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 51 | Active Alarm 3 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 52 | Active Alarm 4 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 53 | Active Alarm 5 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 54 | Active Alarm 6 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 55 | Active Alarm 7 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 56 | Active Alarm 8 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 57 | Active Alarm 9 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 58 | Active Alarm 10 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 59 | Active Alarm 11 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 60 | Active Alarm 12 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 61 | Active Alarm 13 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 62 | Active Alarm 14 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 63 | Active Alarm 15 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 64 | Active Alarm 16 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Active List (A or B). Applicable only for Band or Deviation Alarm Action. |
| 65 | Remote SP Value | -1999 | 9999 | 0 | Read Only |  |
| 66 | Profile Operating Status | 0 | 5 | 0 | Read/Write | 0 = Profile Control Mode Off; Unit will control to active setpoint, 1 = End Profile; Control per profile end action, 2 = Pause, 3 = Error Delay (status only), 4 = Run/Resume/Start, 5 = Advance Profile Segment |
| 67 | Active Profile | 1 | 16 | 1 | Read | (0 = Stop, 1-16 = Current Profile) |
| 68 | Active Segment | 1 | 20 | 1 | Read | (0 = Stop, 1-20 = Current Segment) |
| 69 | Profile Segment Type | 0 | 1 | 0 | Read | 0 = Ramp, 1 = Hold |
| 70 | Active Profile Cycle Count Remaining | 0 | 250 | 0 | Read/Write | 0-250; If Cycle Count is 0 unit is configured for continuous cycling |
| 71 | Active Profile Segment Time Remaining (Hi Word) | 0 | 9999 | N/A | Read/Write | 1 = 0.1 Minute; Can make temporary change on the fly, however, if Active Profile Segment's Time resolution is in minutes, the least significant |
| 72 | Active Profile Segment Time Remaining (Lo Word) | 0 | 9999 | N/A | Read/Write | decade is ignored (i.e., $38=30$ minutes) |
| 73 | Profile Event Status | 0 | 15 | 0 | Read/Write | Bit 3 = Event 4, Bit 2 = Event 3, Bit 1 = Event 2; Bit 0 = Event 1 |


| REGISTER ADDRESS | REGISTER NAME | LOW LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| INPUT PARAMETERS |  |  |  |  |  | SEE INPUT MODULE FOR PARAMETER DESCRIPTIONS |  |  |
| Analog Input Parameters |  |  |  |  |  |  |  |  |
| 101 | Input Range | 0 | 26 | 16 | Read/Write | $0=250 \mu \mathrm{~A}$ $5=250 \mathrm{mV}$ $11=100 \Omega$ $17=$ TC-K $23=$ RTD 385  <br> $1=2.5 \mathrm{~mA}$ $6=2 \mathrm{~V}$ $12=1 \mathrm{~K} \Omega$ $18=$ TC-R $24=$ RTD 392  <br> $2=25 \mathrm{~mA}$ $7=10 \mathrm{~V}$ $13=10 \mathrm{~K} \Omega$ $19=$ TC-S $25=$ RTD 672  <br> $3=250 \mathrm{~mA}$ $8=25 \mathrm{~V}$ $14=$ TC-T $20=$ TC-B $26=$ RTD 427  <br> $4=2 \mathrm{~A}$ $9=100 \mathrm{~V}$ $15=$ TC-E $21=$ TC-N   <br>  $10=200 \mathrm{~V}$ $16=$ TC-J $22=$ TC-C   <br>  10     |  |  |
| 102 | Square Root Linearization | 0 | 1 | 0 | Read/Write | $0=$ No, $1=$ Yes (Valid on Process Inputs) |  |  |
| 103 | Temperature Scale (TC or RTD only) | 0 | 1 | 1 | Read/Write | $0={ }^{\circ} \mathrm{C}, 1={ }^{\circ} \mathrm{F}$ |  |  |
| 104 | Ice Point Compensation (TC only) | 0 | 1 | 1 | Read/Write | $0=$ Off, $1=$ On |  |  |
| 105 | ADC Conversion Rate (samples/sec) | 0 | 5 | 2 | Read/Write | $0=5,1=10,2=20,3=40,4=80,5=160$ |  |  |
| 106 | Decimal Point | 0 | 3 | 1 | Read/Write | $0=0,1=0.0,2=0.00,3=0.000$ |  |  |
| 107 | Rounding Factor | 0 | 6 | 0 | Read/Write | $0=1,1=2,2=5,3=10,4=20,5=50,6=100$ |  |  |
| 108 | Input Offset Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |  |  |
| 109 | Digital Input Filter | 0 | 250 | 10 | Read/Write | 1 = 0.1 Second |  |  |
| 110 | Input Scaling Points in List Function | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1=\mathrm{Yes}$ |  |  |
| 111 | Display Input Units | 0 | 1 | 1 | Read/Write | $0=$ No, 1 = Yes |  |  |
| 112 | Input Units Character 1 | 0 | 57 | 0 | Read/Write |  | $\begin{array}{ll} Z & 36=8 \\ 0 & 37=9 \\ 1 & 38=a \\ 2 & 39=c \\ 3 & 40=e \\ 4 & 41=\mathrm{g} \\ 5 & 42=\mathrm{h} \\ 6 & 43=\mathrm{i} \\ 7 & 44=\mathrm{n} \end{array}$ | $\begin{array}{ll} 45=\mathrm{m}(\mathrm{r}) & 54=] \\ 46=0 & 55=/ \\ 47=\mathrm{q} & 56=0 \\ 48=\mathrm{r} & 57=- \\ 49=\mathrm{u} & \\ 50=\mathrm{w}(\mathrm{r}) & \\ 51=- & \\ 52== & \\ 53=[ & \\ \hline \end{array}$ |
| 113 | Input Units Character 2 |  |  | 56 | Read/Write | See Input Units Character 1 |  |  |
| 114 | Input Units Character 3 |  |  | 6 | Read/Write | See Input Units Character 1 |  |  |
| User Input / Function Keys |  |  |  |  |  |  |  |  |
| 151 | User Input Active State | 0 | 1 | 0 | Read/Write | 0 = Active Low, 1 = Active High |  |  |
| 152 | User Input 1 Action | 0 | 29* | 0 | Read/Write | $0=\mathrm{NONE}$ $7=\mathrm{SPrP}$ $14=\mathrm{dLEV}$ <br> $1=\mathrm{PLOC}$ $8=\mathrm{d}-\mathrm{HI}$ $15=\mathrm{dISP}$ <br> $2=\mathrm{ILOC}$ $9=\mathrm{r}-\mathrm{HI}$ $16=\mathrm{LISt}$ <br> $3=\operatorname{trnF}$ $10=\mathrm{d}-\mathrm{Lo}$ $17=\mathrm{Prnt}$ <br> $4=\mathrm{SPSL}$ $11=\mathrm{r}-\mathrm{Lo}$ $18=\mathrm{RnSt}$ <br> $5=\mathrm{RSPt}$ $12=\mathrm{r}-\mathrm{HL}$ $19=\mathrm{PlrS}$ <br> $6=\mathrm{PSEL}$ $13=\mathrm{r}-\mathrm{AL}$ $20=\mathrm{PlrH}$ | $\begin{aligned} & 21=\mathrm{PrrS} \\ & 22=\mathrm{PrrH} \\ & 23=\text { PStr } \\ & 24=\mathrm{Adnc} \\ & 25=\text { PAUS } \\ & 26=\text { PEnd } \\ & 27=r-E v \end{aligned}$ | $\begin{aligned} & 28=\text { NA }-1 \\ & 29=\text { NA }-2 \\ & 30+=\text { FC Functions } \end{aligned}$ |
| 153 | User Input 1 Alarm Mask | 0 | 65535 | 0 | Read/Write |  |  |  |
| 154 | User Input 2 Action | 0 | 29* | 0 | Read/Write | Same as User Input 1 Action |  |  |
| 155 | User Input 2 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as User Input 1 Alarm Mask |  |  |
| 156 | User F1 Key Action | 0 | 26* | 0 | Read/Write | $0=\mathrm{NONE}$ $6=\mathrm{SPrP}$ $12=\mathrm{dISP}$ $18=\mathrm{PrrS}$ $24=\mathrm{r}-\mathrm{Ev}$ <br> $1=\mathrm{ILOC}$ $7=r-\mathrm{HI}$ $13=\mathrm{LISt}$ $19=\mathrm{PrrH}$ $25=\mathrm{NA}-1$ <br> $2=\operatorname{trnF}$ $8=\mathrm{r}-\mathrm{Lo}$ $14=\mathrm{Prnt}$ $20=\mathrm{PS}$ tr $26=\mathrm{NA}-2$ <br> $3=\mathrm{SPSL}$ $9=r-\mathrm{HL}$ $15=\mathrm{RnSt}$ $21=\mathrm{Adnc}$ $27+=\mathrm{FC}$ Functions <br> $4=\mathrm{RSPt}$ $10=\mathrm{r}-\mathrm{AL}$ $16=\mathrm{PlrS}$ $22=\mathrm{PAUS}$  <br> $5=\mathrm{PSEL}$ $11=\mathrm{dLEV}$ $17=\mathrm{PlrH}$ $23=$ PEnd  |  |  |
| 157 | User F1 Key Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as User Input 1 Alarm Mask |  |  |


| REGISTER ADDRESS | REGISTER NAME | LOW <br> LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 158 | User F2 Key Action | 0 | 26* | 0 | Read/Write | Same as User F1 Key Action |
| 159 | User F2 Key Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as User Input 1 Alarm Mask |
| 160 | User F1 Second Action | 0 | 26* | 0 | Read/Write | Same as User F1 Key Action |
| 161 | User F1 Second Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as User Input 1 Alarm Mask |
| 162 | User F2 Second Action | 0 | 26* | 0 | Read/Write | Same as User F1 Key Action |
| 163 | User F2 Second Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as User Input 1 Alarm Mask |
| Advanced Input Parameters |  |  |  |  |  |  |
| List A | Input Scaling Points Parameters |  |  |  |  |  |
| 171 | Number of Scaling Points | 2 | 16 | 2 | Read/Write | Number of Linearization Scaling Points |
| 172 | Reserved | N/A | N/A | N/A | N/A |  |
| 173 | Scaling Pt. 1 Input Value | -1999 | 9999 | 0 | Read/Write | 1 = 0.001 |
| 174 | Scaling Pt. 1 Display Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 175 215 | Scaling Pt. 2 Input Value | -1999 | 9999 | 1000 | Read/Write | 1 = 0.001 |
| 176 | Scaling Pt. 2 Display Value | -1999 | 9999 | 1000 | Read/Write | 1 = 1 Display Unit |
| 177 thru 217 thru <br> 202 242 <br> 203 243 | Scaling Pts. 3 thru 15 Values | -1999 | 9999 | 0 | Read/Write | Registers 40177-40202 and 40217-40242 hold values for Scaling Points 3 thru 15, and follow the same ordering as Scaling Point 1. |
| $203-243$ | Scaling Pt. 16 Input Value | -1999 | 9999 | 0 | Read/Write | 1 = 0.001 |
| 204 | Scaling Pt. 16 Display Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| OUTPUT PARAMETERS |  |  |  |  |  |  |
| 251 | Output 1 Assignment | 0 | 23* | 1 | Read/Write | $0=$ NONE $7=$ RSPt $14=$ PHLd $21=$ PEv4 <br> $1=\mathrm{HEAt}$ $8=\mathrm{ILOC}$ $15=$ PAUS $22=\mathrm{NA}-1$ <br> $2=\mathrm{COOL}$ $9=\mathrm{tunE}$ $16=$ PErb $23=$ NA -2 <br> $3=$ ALr $10=\mathrm{tndn}$ $17=$ PErt $24+=$ FlexCard <br> $4=$ MAN $11=\mathrm{tnFL}$ $18=$ PEv1 Assignments <br> $5=$ SPSL $12=$ PCtL $19=$ PEv2  <br> $6=$ SPrP $13=$ Prun $20=$ PEv3  |
| 252 | Output 1 Logic/Alarm Logic Mode | 0 | 2 | 0 | Read/Write | If Out Assignment $\neq$ ALr; $0=$ NOR, $1=$ REV <br> If Output Assignment = ALr; $0=$ SINGLE, $1=$ AND, $2=\mathrm{OR}$ |
| 253 | Output 1 Alarm Mask | 0 | 65535 | 0 | Read/Write | Bit $0=$ A1 Bit $4=$ A5 Bit $8=$ A9 Bit $12=$ A13 <br> Bit 1 = A2 Bit $5=$ A6 Bit $9=$ A10 Bit 13 $=$ A14 <br> Bit 2 =A3 Bit $6=$ A7 Bit 10 $=$ A11 Bit 14 $=$ A15 <br> Bit 3 =A4 Bit 7 =A8 Bit 11=A12 Bit 15 =A16 |
| 254 | Output 1 Cycle Time | 0 | 600 | 20 | Read/Write | 1 = 0.1 Second |
| 255 | Output 2 Assignment | 0 | 23* | 0 | Read/Write | Same as Output 1 Assignment |
| 256 | Output 2 Logic/Alarm Logic Mode | 0 | 2 | 0 | Read/Write | Same as Output 1 Logic/Alarm Logic Mode |
| 257 | Output 2 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Output 1 Alarm Mask |
| 258 | Output 2 Cycle Time | 0 | 600 | 20 | Read/Write | 1 = 0.1 Second |
| 259 | Output 3 Assignment | 0 | 23* | 0 | Read/Write | Same as Output 1 Assignment |
| 260 | Output 3 Logic/Alarm Logic Mode | 0 | 2 | 0 | Read/Write | Same as Output 1 Logic/Alarm Logic Mode |
| 261 | Output 3 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Output 1 Alarm Mask |
| 262 | Output 3 Cycle Time | 0 | 600 | 20 | Read/Write | 1 = 0.1 Second |
| 263 | Output 4 Assignment | 0 | 23* | 0 | Read/Write | Same as Output 1 Assignment |
| 264 | Output 4 Logic/Alarm Logic Mode | 0 | 2 | 0 | Read/Write | Same as Output 1 Logic/Alarm Logic Mode |
| 265 | Output 4 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Output 1 Alarm Mask |
| 266 | Output 4 Cycle Time | 0 | 600 | 20 | Read/Write | 1 = 0.1 Second |
| Analog Output |  |  |  |  |  |  |
| 271 | Non-Linear Analog Output Scaling | 0 | 1 | 0 | Read/Write | $0=$ No, 1 = Yes (Use Non-Linear Analog Output Scaling Parameters) |
| 272 | Type | 0 | 2 | 1 | Read/Write | $0=0-20 \mathrm{~mA}, 1=4-20 \mathrm{~mA}, 2=0-10 \mathrm{~V}$ |
| 273 | Assignment | 0 | 6* | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{PV}, 2=\mathrm{HI}, 3=\mathrm{LO}, 4=\mathrm{OP}, 5=\mathrm{SP}(\text { Active }), 6=\mathrm{dEv} \text {, } \\ & 7+=\text { FlexCard Assignments } \end{aligned}$ |
| 274 | Analog Low Scale Value | -1999 | 9999 | 0 | Read/Write | Display value that corresponds with $0 \mathrm{~V}, 0 \mathrm{~mA}$ or 4 mA output |
| 275 | Analog High Scale Value | -1999 | 9999 | 1000 | Read/Write | Display value that corresponds with 10 V or 20 mA output |



| REGISTER ADDRESS | REGISTER NAME | LOW LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 304 | Line 1 Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 305 | Line 1 Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| 306 | Line 1 Red Backlight Assignment | 0 | $25^{*}$ | 0 | Read/Write | Same as Line 1 Green Backlight Assignment |
| 307 | Line 1 Red Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 308 | Line 1 Red Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| 309 | Line 1 Green-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Line 1 Green Backlight Assignment |
| 310 | Line 1 Green-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 311 | Line 1 Green-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| 312 | Line 1 Red-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Line 1 Green Backlight Assignment |
| 313 | Line 1 Red-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 314 | Line 1 Red-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| 315 | Line 1 Red-Green Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Line 1 Green Backlight Assignment |
| 316 | Line 1 Red-Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 317 | Line 1 Red-Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| Line 2 |  |  |  |  |  |  |
| 331 | Line 2 Default Display Color | 0 | 2 | 0 | Read/Write | 0 = Grn, 1 = OrNG, 2 = rEd |
| 332 | Deprecated |  |  |  |  | See registers 111-114 for Input Unit's programming |
| 333 | Deprecated |  |  |  |  | See registers 111-114 for Input Unit's programming |
| 334 | Deprecated |  |  |  |  | See registers 111-114 for Input Unit's programming |
| 335 | Deprecated |  |  |  |  | See registers 111-114 for Input Unit's programming |
| 336 | Line 2 Bargraph Assignment | 0 | 6* | 2 | Read/Write | $\begin{aligned} & 0=\text { NONE, } \quad 1=\mathrm{OP}, \quad 2=\mathrm{dEv}, \quad 3=\mathrm{SP}, \quad 4=\mathrm{OP} \text { ANy, } \quad 5=\mathrm{dEv} \mathrm{ANy}, \\ & 6=\text { SP ANy }, \quad 7+=\text { FlexCard Assignments } \end{aligned}$ |
| 337 | Line 2 Bargraph Low Scale Value | 0 | 9999 | 0 | Read/Write |  |
| 338 | Line 2 Bargraph High Scale Value | 0 | 9999 | 100 | Read/Write |  |
| 339 | Line 2 Green Backlight Assignment | 0 | 25* | 0 | Read/Write | $0=$ NONE $5=\mathrm{ALr}$ $10=\mathrm{ILOC}$ $15=$ Prun $20=$ PEv1 $25=\mathrm{NA}-2$ <br> $1=$ Out1 $6=$ MAN $11=$ tunE $16=$ PHLd $21=$ PEv2 <br> $26+=$ FlexCard     <br> $2=$ Out2 $7=$ SPSL $12=$ tndn $17=$ PAUS $22=$ PEv3 <br> A Assignments     <br> = Out3 $8=$ SPrP $13=$ tnFL $18=$ PErb $23=$ PEv4 |
| 340 | Line 2 Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 341 | Line 2 Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write |  |
| 342 | Line 2 Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Line 2 Green Backlight Assignment |
| 343 | Line 2 Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 344 | Line 2 Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 2 Green Backlight Alarm Mask |
| 345 | Line 2 Red Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Line 2 Green Backlight Assignment |
| 346 | Line 2 Red Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 347 | Line 2 Red Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 2 Green Backlight Alarm Mask |
| 348 | Line 2 Green-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Line 2 Green Backlight Assignment |
| 349 | Line 2 Green-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 350 | Line 2 Green-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 2 Green Backlight Alarm Mask |
| 351 | Line 2 Red-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Line 2 Green Backlight Assignment |
| 352 | Line 2 Red-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 353 | Line 2 Red-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 2 Green Backlight Alarm Mask |
| 354 | Line 2 Red-Green Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Line 2 Green Backlight Assignment |
| 355 | Line 2 Red-Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 356 | Line 2 Red-Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 2 Green Backlight Alarm Mask |



| REGISTER ADDRESS | REGISTER NAME | LOW LIMIT | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 397 | UA 2 Assignment Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 398 | UA 2 Assignment Alarm Mask | 0 | 65535 | 1 | Read/Write |  |
| 399 | UA 2 Green Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 2 Units Assignment |
| 400 | UA 2 Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 401 | UA 2 Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 2 Assignment Alarm Mask |
| 402 | UA 2 Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 2 Units Assignment |
| 403 | UA 2 Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 404 | UA 2 Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 2 Assignment Alarm Mask |
| 405 | UA 2 Red Backlight Assignment | 0 | $25^{*}$ | 5 | Read/Write | Same as UA 2 Units Assignment |
| 406 | UA 2 Red Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 407 | UA 2 Red Backlight Alarm Mask | 0 | 65535 | 1 | Read/Write | Same as UA 2 Assignment Alarm Mask |
| 408 | UA 2 Green-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 2 Units Assignment |
| 409 | UA 2 Green-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 410 | UA 2 Green-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 2 Assignment Alarm Mask |
| 411 | UA 2 Red-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 2 Units Assignment |
| 412 | UA 2 Red-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 413 | UA 2 Red-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 2 Assignment Alarm Mask |
| 414 | UA 2 Red-Green Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 2 Units Assignment |
| 415 | UA 2 Red-Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 416 | UA 2 Red-Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 2 Assignment Alarm Mask |
| Universal Annunciator 3 |  |  |  |  |  |  |
| 421 | UA 3 Default Display Color | 0 | 2 | 0 | Read/Write | $0=$ Grn, 1 = OrNG, $2=$ rEd |
| 422 | UA 3 Units Mnemonic | 0 | 1 | 1 | Read/Write | 0 = Off, 1 = On |
| 423 | UA 3 Units Digit 1 (Left) | 0 | 57 | 1 | Read/Write | Same as UA1 Units Selection |
| 424 | UA 3 Units Digit 2 (Right) | 0 | 57 | 30 | Read/Write |  |
| 425 | UA 3 Units Logic Mode (Active) | 0 | 2 | 0 | Read/Write | 0 = nor, 1 = rEv, 2 = FLSh |
| 426 | UA 3 Units Assignment | 0 | 25* | 5 | Read/Write | $0=$ NONE $5=\mathrm{ALr}$ $10=\mathrm{ILOC}$ $15=$ Prun $20=\mathrm{PEv} 1$ $25=\mathrm{NA}-2$  <br> $1=$ Out 1 $6=\mathrm{MAN}$ $11=$ tunE $16=$ PHLd $21=$ PEv2 $26+=$ FlexCard <br> $2=$ Out2 $7=$ SPSL $12=$ tndn $17=$ PAUS $22=$ PEv3 Assignments <br> $3=$ Out3 $8=$ SPrP $13=$ tnFL $18=$ PErb $23=$ PEv4  <br> $4=$ Out4 $9=$ RSPt $14=$ PCtL $19=$ PErt $24=$ NA- 1  |
| 427 | UA 3 Assignment Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 428 | UA 3 Assignment Alarm Mask | 0 | 65535 | 2 | Read/Write | Bit $0=$ A1 Bit $4=$ A5 Bit $8=$ A9 Bit 12 $=$ A13 <br> Bit 1 = A2 Bit $5=$ A6 Bit $9=$ A10 Bit 13 $=$ A14 <br> Bit 2 =A3 Bit $6=$ A7 Bit 10 $=$ A11 Bit 14 $=$ A15 <br> Bit 3 =A4 Bit $7=$ A8 Bit 11 =A12 Bit 15 =A16 |
| 429 | UA 3 Green Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 3 Units Assignment |
| 430 | UA 3 Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 431 | UA 3 Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 3 Assignment Alarm Mask |
| 432 | UA 3 Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 3 Units Assignment |
| 433 | UA 3 Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 434 | UA 3 Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 3 Assignment Alarm Mask |
| 435 | UA 3 Red Backlight Assignment | 0 | 25** | 5 | Read/Write | Same as UA 3 Units Assignment |
| 436 | UA 3 Red Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 437 | UA 3 Red Backlight Alarm Mask | 0 | 65535 | 2 | Read/Write | Same as UA 3 Assignment Alarm Mask |
| 438 | UA 3 Green-Orange Backlight Assignment | 0 | 25 | 0 | Read/Write | Same as UA 3 Units Assignment |
| 439 | UA 3 Green-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 440 | UA 3 Green-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 3 Assignment Alarm Mask |
| 441 | UA 3 Red-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 3 Units Assignment |


| REGISTER ADDRESS | REGISTER NAME | $\begin{aligned} & \hline \text { LOW } \\ & \text { LIMIT } \end{aligned}$ | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 442 | UA 3 Red-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | $0=$ SINGLE, 1 = AND, $2=$ OR |  |  |  |
| 443 | UA 3 Red-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 3 Assignment Alarm Mask |  |  |  |
| 444 | UA 3 Red-Green Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 3 Units Assignment |  |  |  |
| 445 | UA 3 Red-Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |  |  |  |
| 446 | UA 3 Red-Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 3 Assignment Alarm Mask |  |  |  |
| Universal Annunciator 4 |  |  |  |  |  |  |  |  |  |
| 451 | UA 4 Default Display Color | 0 | 2 | 0 | Read/Write | $0=\mathrm{Grn}, 1$ = OrNG, 2 = rEd |  |  |  |
| 452 | UA 4 Units Mnemonic | 0 | 1 | 0 | Read/Write | $0=$ Off, 1 = On |  |  |  |
| 453 | UA 4 Units Digit 1 (Left) | 0 | 57 | 0 | Read/Write | Same as UA1 Units Selection |  |  |  |
| 454 | UA 4 Units Digit 2 (Right) | 0 | 57 | 0 | Read/Write |  |  |  |  |
| 455 | UA 4 Units Logic Mode (Active) | 0 | 2 | 0 | Read/Write | $0=$ nor, 1 = rEv, $2=\mathrm{FLSh}$ |  |  |  |
| 456 | UA 4 Units Assignment | 0 | 25* | 0 | Read/Write | $0=$ NONE $5=$ ALr $10=\mathrm{ILOC}$ $15=$ Prun $20=$ PEv1 $25=$ NA-2 <br> $1=$ Out1 $6=$ MAN $11=$ tunE $16=$ PHLd $21=$ PEv2 $26+=$ FlexCard <br> $2=$ Out2 $7=$ SPSL $12=$ tndn $17=$ PAUS $22=$ PEv3 Assignments <br> $3=$ Out3 $8=$ SPrP $13=$ tnFL $18=$ PErb $23=$ PEv4  <br> $4=$ Out4 $9=$ RSPt $14=$ PCtL $19=$ PErt $24=$ NA-  |  |  |  |
| 457 | UA 4 Assignment Alarm Logic Mode | 0 | 2 | 0 | Read/Write | $0=$ SINGLE, 1 = AND, $2=$ OR |  |  |  |
| 458 | UA 4 Assignment Alarm Mask | 0 | 65535 | 0 | Read/Write | Bit $0=$ A1 Bit $4=$ A5 Bit $8=$ A9 Bit $12=$ A13 <br> Bit 1 $=$ A2 Bit $5=$ A6 Bit $9=$ A10 Bit 13 $=$ A14 <br> Bit $2=$ A3 Bit $6=$ A7 Bit 10 $=$ A11 Bit 14 $=$ A15 <br> Bit 3 =A4 Bit 7 7 A 8 Bit 11 $=$ A12 Bit 15 =A16 |  |  |  |
| 459 | UA 4 Green Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 4 Units Assignment |  |  |  |
| 460 | UA 4 Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | $0=$ SINGLE, 1 = AND, $2=0 \mathrm{O}$ |  |  |  |
| 461 | UA 4 Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 4 Assignment Alarm Mask |  |  |  |
| 462 | UA 4 Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 4 Units Assignment |  |  |  |
| 463 | UA 4 Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |  |  |  |
| 464 | UA 4 Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 4 Assignment Alarm Mask |  |  |  |
| 465 | UA 4 Red Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 4 Units Assignment |  |  |  |
| 466 | UA 4 Red Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, $2=$ OR |  |  |  |
| 467 | UA 4 Red Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 4 Assignment Alarm Mask |  |  |  |
| 468 | UA 4 Green-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 4 Units Assignment |  |  |  |
| 469 | UA 4 Green-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | $0=$ SINGLE, 1 = AND, $2=0 \mathrm{R}$ |  |  |  |
| 470 | UA 4 Green-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 4 Assignment Alarm Mask |  |  |  |
| 471 | UA 4 Red-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 4 Units Assignment |  |  |  |
| 472 | UA 4 Red-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |  |  |  |
| 473 | UA 4 Red-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 4 Assignment Alarm Mask |  |  |  |
| 474 | UA 4 Red-Green Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as UA 4 Units Assignment |  |  |  |
| 475 | UA 4 Red-Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | $0=$ SINGLE, 1 = AND, $2=$ OR |  |  |  |
| 476 | UA 4 Red-Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as UA 4 Assignment Alarm Mask |  |  |  |
| Mnemonics |  |  |  |  |  |  |  |  |  |
| 501 | Mnemonic Default Display Color | 0 | 2 | 0 | Read/Write | $0=\mathrm{Grn}, 1$ = OrNG, 2 = rEd |  |  |  |
| 502 | Mnemonic Green Backlight Assignment | 0 | 25* | 0 | Read/Write | $0=$ NONE $5=$ ALr $10=\mathrm{ILOC}$ $15=$ Prun $20=$ PEv1 $25=$ NA-2 <br> $1=$ Out1 $6=$ MAN $11=$ tunE $16=$ PHLd $21=$ PEv2 <br> $26+=$ FlexCard     <br> $2=$ Out2 $7=$ SPSL $12=$ tndn $17=$ PAUS $22=$ PEv3 <br> $3=$ Out3 $8=$ SPrP $13=$ tnFL $18=$ PErb $23=$ PEv4 |  |  |  |
| 503 | Mnemonic Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | $0=$ SINGLE, 1 = AND, $2=0 \mathrm{O}$ |  |  |  |
| 504 | Mnemonic Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Bit $0=$ A1 Bit $4=$ A5 Bit $8=$ A9 Bit $12=$ A13 <br> Bit $1=$ A2 Bit $5=$ A6 Bit $9=$ A10 Bit 13 A14 <br> Bit 2 A A3 Bit $6=$ A7 Bit 10 A11 Bit 14 =A15 <br> Bit 3 =A4 Bit $7=$ A8 Bit 11 =A12 Bit 15 = A16 |  |  |  |
| 505 | Mnemonic Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Mnemonic Gree | n Backlight As | signment |  |


| REGISTER ADDRESS | REGISTER NAME | LOW LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
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| 506 | Mnemonic Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 507 | Mnemonic Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| 508 | Mnemonic Red Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Mnemonic Green Backlight Assignment |
| 509 | Mnemonic Red Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 510 | Mnemonic Red Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| 511 | Mnemonic Green-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Mnemonic Green Backlight Assignment |
| 512 | Mnemonic Green-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 513 | Mnemonic Green-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| 514 | Mnemonic Red-Orange Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Mnemonic Green Backlight Assignment |
| 515 | Mnemonic Red-Orange Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 516 | Mnemonic Red-Orange Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| 517 | Mnemonic Red-Green Backlight Assignment | 0 | 25* | 0 | Read/Write | Same as Mnemonic Green Backlight Assignment |
| 518 | Mnemonic Red-Green Backlight Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 519 | Mnemonic Red-Green Backlight Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Line 1 Green Backlight Alarm Mask |
| Line 2 Profile LOCS |  |  |  |  |  |  |
| 531 | Line 2 Profile Control Status Access | 0 | 21 | 0 | Read/Write | 0 = LOC; Bit 0 = drEd, Bit 2 = PrEd, Bit4 = HrEd; Other bits N/A |
| 532 | Line 2 Profile Segment Time Remaining Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 533 | Line 2 Profile Cycle Count Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 534 | Line 2 Profile Programming Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{aligned}$ |
| Line 2 Display LOCS |  |  |  |  |  |  |
| 541 | Line 2 Input Display Access | 0 | 21 | 0 | Read/Write | 0 = LOC; Bit $0=$ drEd, Bit 2 = PrEd, Bit4 = HrEd; Other bits N/A |
| 542 | Line 2 Maximum (Hi) Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 543 | Line 2 Minimum (Lo) Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| Line 2 Display LOCS |  |  |  |  |  |  |
| 551 | Display Intensity Level Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 552 | Display Contrast Level Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{aligned}$ |
| Line 2 Alarm LOCS |  |  |  |  |  |  |
| 561 | Line 2 Alarm 1 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 562 | Line 2 Alarm 1 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 563 | Line 2 Alarm 2 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{aligned}$ |
| 564 | Line 2 Alarm 2 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 565 | Line 2 Alarm 3 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 566 | Line 2 Alarm 3 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 567 | Line 2 Alarm 4 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{aligned}$ |
| 568 | Line 2 Alarm 4 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |


| REGISTER ADDRESS | REGISTER NAME | LOW LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 569 | Line 2 Alarm 5 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{array} \end{aligned}$ |
| 570 | Line 2 Alarm 5 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{array}{\|l} \hline 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{array}$ |
| 571 | Line 2 Alarm 6 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1 \text { = dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 572 | Line 2 Alarm 6 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \hline \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{array} \\ & \hline \end{aligned}$ |
| 573 | Line 2 Alarm 7 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{array} \end{aligned}$ |
| 574 | Line 2 Alarm 7 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ \text { Bit4 } 4 \text { HrEd, Bit5 = HEnt } \end{array} \\ & \hline \end{aligned}$ |
| 575 | Line 2 Alarm 8 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1 \text { = dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ \text { Bit4 = HrEd, Bit5 = HEnt } \end{array} \end{aligned}$ |
| 576 | Line 2 Alarm 8 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ \text { Bit4 } 4 \text { HrEd, Bit5 = HEnt } \end{array} \\ & \hline \end{aligned}$ |
| 577 | Line 2 Alarm 9 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1 \text { = dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 578 | Line 2 Alarm 9 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 579 | Line 2 Alarm 10 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \hline \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{array} \\ & \hline \end{aligned}$ |
| 580 | Line 2 Alarm 10 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 581 | Line 2 Alarm 11 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \hline 0=\text { LOC; Bit } 0 \text { = drEd, Bit } 1 \text { = dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 582 | Line 2 Alarm 11 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1 \text { = dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 583 | Line 2 Alarm 12 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{array} \end{aligned}$ |
| 584 | Line 2 Alarm 12 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ \text { Bit4 } 4 \text { HrEd, Bit5 = HEnt } \end{array} \\ & \hline \end{aligned}$ |
| 585 | Line 2 Alarm 13 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \hline 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 586 | Line 2 Alarm 13 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{array} \end{aligned}$ |
| 587 | Line 2 Alarm 14 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{array} \\ & \hline \end{aligned}$ |
| 588 | Line 2 Alarm 14 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1 \text { = dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 589 | Line 2 Alarm 15 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{aligned}$ |
| 590 | Line 2 Alarm 15 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{array} \\ & \hline \end{aligned}$ |
| 591 | Line 2 Alarm 16 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1 \text { = dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 592 | Line 2 Alarm 16 Band/Dev.Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{array} \end{aligned}$ |
| Line 2 PID LOCS |  |  |  |  |  |  |
| 601 | Line 2 Actual Setpoint Value Access | 0 | 42 | 2 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{aligned}$ |
| 602 | Line 2 Setpoint 1 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{array} \end{aligned}$ |


| REGISTER ADDRESS | REGISTER NAME | LOW <br> LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 603 | Line 2 Setpoint 2 Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 604 | Line 2 Setpoint List | 0 | 40 | 0 | Read/Write | 0 = LOC; Bit 3 = PEnt, Bit5 = HEnt |
| 605 | Line 2 Remote Setpoint Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 606 | Line 2 Output Power Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 607 | Line 2 Deviation Value Access | 0 | 42 | 0 | Read/Write | 0 = LOC; Bit $0=$ drEd, Bit $2=$ PrEd, Bit4 $=$ HrEd |
| 608 | Line 2 Setpoint Ramp Rate Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 609 | Line 2 Remote Setpoint Ratio Value Access | 0 | 42 | 0 | Read/Write | 0 = LOC, 1 = drEd, 2 = dEnt, 3 = PrEd, 4 = PEnt, 5 = HrEd, 6 = HEnt |
| 610 | Line 2 Remote Setpoint Bias Value Access | 0 | 42 | 0 | Read/Write | 0 = LOC, 1 = drEd, $2=\mathrm{dEnt}, 3=\mathrm{PrEd}, 4=\mathrm{PEnt}, 5$ = HrEd, $6=$ HEnt |
| 611 | Line 2 Actual Offset Power Value Access | 0 | 42 | 0 | Read/Write | 0 = LOC, 1 = drEd, 2 = dEnt, 3 = PrEd, 4 = PEnt, 5 = HrEd, 6 = HEnt |
| 612 | Line 2 Actual Proportional Band Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 613 | Line 2 Actual Integral Time Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 614 | Line 2 Actual Derivitive Time Value Access | 0 | 42 | 0 | Read/Write | $0=$ LOC; Bit $0=$ drEd, Bit $1=\mathrm{dEnt}$, Bit $2=$ PrEd, Bit $3=$ PEnt, Bit4 $=\mathrm{HrEd}$, Bit5 $=$ HEnt |
| 615 | Line 2 PS1 Offset Power Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 616 | Line 2 PS1 Proportional Band Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1 \text { = dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 617 | Line 2 PS1 Integral Time Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 618 | Line 2 PS1 Derivitive Time Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 619 | Line 2 PS2 Offset Power Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 620 | Line 2 PS2 Proportional Band Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ \text { Bit4 } 4 \text { HrEd, Bit5 = HEnt } \end{array} \end{aligned}$ |
| 621 | Line 2 PS2 Integral Time Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 622 | Line 2 PS2 Derivitive Time Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 623 | Line 2 PID Set Selection Value Access | 0 | 40 | 0 | Read/Write | 0 = LOC; Bit 3 = PEnt, Bit5 = HEnt |
| Line 2 Function LOCS |  |  |  |  |  |  |
| 631 | Line 2 Setpoint Selection Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 632 | Line 2 Remote Setpoint Transfer (Local/Remote) | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 633 | Line 2 Setpoint Ramping Disable | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 634 | Line 2 Integral Lock Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 = HEnt } \end{aligned}$ |
| 635 | Line 2 Auto/Manual Mode Selection Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1 \text { = dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 636 | Line 2 PID Bank Selection Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2 \text { = PrEd, Bit } 3 \text { = PEnt, } \\ & \text { Bit4 = HrEd, Bit5 = HEnt } \end{aligned}$ |
| 637 | Line 2 Tune Selection Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & \begin{array}{l} 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3 \text { = PEnt, } \\ \text { Bit4 } 4 \text { HrEd, Bit5 }=\text { HEnt } \end{array} \end{aligned}$ |
| 638 | Line 2 Reset Max Display Access | 0 | 21 | 0 | Read/Write | 0 = LOC; Bit 1 = dEnt, Bit 3 = PEnt, Bit5 = HEnt |
| 639 | Line 2 Reset Min Display Access | 0 | 21 | 0 | Read/Write | 0 = LOC; Bit 1 = dEnt, Bit 3 = PEnt, Bit5 = HEnt |


| REGISTER ADDRESS | REGISTER NAME | $\begin{aligned} & \hline \text { LOW } \\ & \text { LIMIT } \end{aligned}$ | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 640 | Line 2 Reset Max and Min Access | 0 | 21 | 0 | Read/Write | 0 = LOC; Bit 1 = dEnt, Bit $3=$ PEnt, Bit5 $=$ HEnt |
| 641 | Line 2 Reset Alarm Access | 0 | 21 | 0 | Read/Write | 0 = LOC; Bit 1 = dEnt, Bit 3 = PEnt, Bit5 = HEnt |
| 642 | Line 2 List Selection Access | 0 | 42 | 0 | Read/Write | $0=$ LOC; Bit $0=$ drEd, Bit $1=$ dEnt, Bit $2=$ PrEd, Bit $3=$ PEnt, Bit4 = HrEd, Bit5 = HEnt |
| 643 | Line 2 Print Request Access | 0 | 42 | 0 | Read/Write | $0=$ LOC; Bit $0=$ drEd, Bit $1=d E n t$, Bit $2=$ PrEd, Bit $3=$ PEnt, Bit4 $=$ HrEd, Bit5 $=$ HEnt |
| 644 | Line 2 Reset Alarm Mask | 0 | 65535 | 0 | Read/Write | Bit $0=$ A1 Bit $4=$ A5 Bit $8=$ A9 Bit $12=$ A13 <br> Bit $1=$ A2 Bit $5=$ A6 Bit $9=$ A10 Bit 13 $=$ A14 <br> Bit $2=$ A3 Bit $6=$ A7 Bit $10=$ A11 Bit $14=$ A15 <br> Bit $3=$ A4 Bit $7=$ A8 Bit $11=$ A12 Bit 15 $=$ A16 |
| 645 | Line 2 PID Run/Stop Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{aligned}$ |
| 646 | Line 2 Profile Reset Event Access | 0 | 21 | 0 | Read/Write | 0 LOC; Bit 1 = dEnt, Bit 3 = PEnt, Bit5 $=$ HEnt |
| 647 | Line 2 Profile Reset Event Mask | 0 | 15 | 0 | Read/Write | Bit $0=$ Ev1, Bit $1=$ Ev2, Bit $2=$ Ev3, Bit $3=$ Ev4 |
| Max (HI)/Min(LO) Values |  |  |  |  |  |  |
| 651 | Max (HI) Capture Delay Time | 0 | 9999 | 10 | Read/Write | $0=$ Max Update Rate, $1=0.1 \mathrm{Sec}$ |
| 652 | Min (LO) Capture Delay Time | 0 | 9999 | 10 | Read/Write | $0=$ Max Update Rate, $1=0.1 \mathrm{Sec}$ |
| Line 2 Code Configuration |  |  |  |  |  |  |
| 661 | Line 2 Security Code Value | 0 | 250 | 0 | Read/Write |  |
| PID CONFIGURATION PARAMETERS |  |  |  |  |  |  |
| Control |  |  |  |  |  |  |
| 671 | Assign | 0 | 1* | 1 | Read/Write | $0=$ NONE, 1 = PV, 2+ = Flex Card Assignments |
| 672 | Control Type | 0 | 2 | 0 | Read/Write | $0=\mathrm{HEAt}, 1$ = COOL, $2=$ both |
| 673 | Control Mode | 0 | 1 | 0 | Read/Write | $0=$ Auto, 1 = MAN |
| 674 | Manual Power | -1000 | 1000 | 0 | Read/Write | Output Power: Heat/Cool; * writable only in manual mode; $1=0.1 \%$ |
| Remote Setpoint |  |  |  |  |  |  |
| 676 | Remote SP Assignment | 0 | 4* | 0 | Read/Write | $0=$ NONE, $1=$ SP, $2=\mathrm{PV}, 3=\mathrm{OP}, 4=\mathrm{ScSP}, 5+=$ Flex Card Assignments |
| 677 | Reserved for future use. |  |  |  |  |  |
| 678 | Ratio | 1 | 9999 | 1000 | Read/Write | $1=0.1$ |
| 679 | Bias | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 680 | Select Local / Remote SP | 0 | 1 | 0 | Read/Write | 0 = LOC, 1 = REM |
| Setpoint |  |  |  |  |  |  |
| 681 | Setpoint Selection | 0 | 5 | 0 | Read/Write | $0=\mathrm{SP} 1,1$ = SP2, $2=\mathrm{SP} 3,3=\mathrm{SP} 4,4=\mathrm{SP} 5,5=\mathrm{SP6}$, $6=\mathrm{SPu}$ |
| 682 | Sepoint 1 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 683 | Setpoint 2 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 684 | Setpoint Lo Limit Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 685 | Setpoint Hi Limit Value | -1999 | 9999 | 9999 | Read/Write | 1 = 1 Display Unit |
| 686 | Ramp Timebase | 0 | 3 | 0 | Read/Write | $0=$ Off, 1 = Seconds, 2 = Minutes, 3 = Hours |
| 687 | Ramp Rate | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Ramp Timebase unit |
| PID Parameters |  |  |  |  |  |  |
| 691 | PID Parameter Selection | 0 | 1 | 0 | Read/Write | 0 = PS1 PID Values, 1 = Alternate PID Values |
| 692 | PS1 Proportional Band | 0 | 9999 | 700 | Read/Write | 1 = 1 Display Unit |
| 693 | PS1 Integral Time | 0 | 65000 | 120 | Read/Write | $1=0.1$ Second |
| 694 | PS1 Derivative Time | 0 | 9999 | 30 | Read/Write | 1 =0.1 Second |
| 695 | PS1 Power Filter Value | 0 | 600 | 10 | Read/Write | $1=0.1$ Second |
| 696 | PS1 Output Power Offset | -1000 | 1000 | 0 | Read/Write | $1=0.1$ \%; Applicable when PS1 Integral Time is 0 |
| 697 | PS2 Proportional Band | 0 | 9999 | 700 | Read/Write | 1 = 1 Display Unit |
| 698 | PS2 Integral Time | 0 | 65000 | 120 | Read/Write | 1 = 0.1 Second |
| 699 | PS2 Derivative Time | 0 | 9999 | 30 | Read/Write | 1 = 0.1 Second |
| 700 | PS2 Power Filter Value | 0 | 600 | 10 | Read/Write | $1=0.1$ Second |
| 701 | PS2 Output Power Offset | -1000 | 1000 | 0 | Read/Write | 1 = 0.1 \%; Applicable when PS2 Integral Time is 0 |


| REGISTER ADDRESS | REGISTER NAME | LOW <br> LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power Transfer |  |  |  |  |  |  |
| 711 | Input Fault Power Value | -1999 | 2000 | 0 | Read/Write | 1 = 0.1 \% |
| 712 | Output Deadband | -1000 | 1000 | 0 | Read/Write | 1 = 0.1 \% |
| 713 | Output Heat Gain | 0 | 5000 | 1000 | Read/Write | 1 = 0.1 \% |
| 714 | Heat Low Limit | 0 | 2000 | 0 | Read/Write | 1 = 0.1 \% |
| 715 | Heat High Limit | 0 | 2000 | 1000 | Read/Write | 1 = 0.1 \% |
| 716 | Output Cool Gain | 0 | 5000 | 1000 | Read/Write | 1 = 0.1 \% |
| 717 | Cool Low Limit | 0 | 2000 | 0 | Read/Write | 1 = 0.1 \% |
| 718 | Cool High Limit | 0 | 2000 | 1000 | Read/Write | 1 = 0.1 \% |
| ON/OFF Control |  |  |  |  |  |  |
| 741 | On-Off Hysteresis | 0 | 500 | 2 | Read/Write | 1 = 1 Display Unit |
| 742 | On-Off Deadband | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| Tuning |  |  |  |  |  |  |
| 751 | Tuning Code | 0 | 4 | 2 | Read/Write | $\begin{aligned} & 0=\text { Very Aggressive, } 1 \text { = Aggressive, } 2 \text { = Default, } 3 \text { = Conservative, } \\ & 4=\text { Very Conservative } \end{aligned}$ |
| 752 | Auto-Tune Start | 0 | 1 | 0 | Read/Write | 0 = NO 1 = YES |
| PID Setpoints |  |  |  |  |  |  |
| 761 | Setpoint 1 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit (Mirrors Register 682) |
| 762 | Setpoint 2 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit (Mirrors Register 683) |
| 763 | Setpoint 3 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 764 | Setpoint 4 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 765 | Setpoint 5 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 766 | Setpoint 6 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 767 | User Setpoint Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| PID Constants Sets (PSn) |  |  |  |  |  |  |
| 801-807 | SP1 / PID Set PS1 Constants |  |  |  |  | Mirrors PS1 PID Constants, registers 692-696 |
| 801 | Setpoint 1 | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 802 | PS1 Proportional Band | 0 | 9999 | 700 | Read/Write | 1 = 1 Display Unit |
| 803 | PS1 Integral Time | 0 | 65000 | 120 | Read/Write | 1 = 0.1 Second |
| 804 | PS1 Derivative Time | 0 | 9999 | 30 | Read/Write | 1 =0.1 Second |
| 805 | PS1 Power Filter Value | 0 | 600 | 10 | Read/Write | $1=0.1$ Second |
| 806 | PS1 Output Power Offset | -1000 | 1000 | 0 | Read/Write | 1 = 0.1 \%; Applicable when PS1 Integral Time is 0 |
| 807 | PS1 Heat Gain | 0 | 5000 | 1000 | Read/Write | 1 = 0.1 \% |
| 808 | PS1 Cool Gain | 0 | 5000 | 1000 | Read/Write | 1 = 0.1 \% |
| 811-817 | SP2 / PID Set PS2 Constants |  |  |  |  | Same order as SP1 /PID Set PS1 Constants (Register 801-807) |
| 821-827 | SP3 /PID Set PS3 Constants |  |  |  |  |  |
| 831-837 | SP4 /PID Set PS4 Constants |  |  |  |  |  |
| 841-847 | SP5 /PID Set PS5 Constants |  |  |  |  |  |
| 851-857 | SP6 /PID Set PS6 Constants |  |  |  |  |  |
| Slave ID / GUID |  |  |  |  |  |  |
| 1001-1010 | Slave ID | N/A | N/A | N/A | Read Only | ```<'P' 'X'> <'2' 'C'> <'1' '5'> <2020h> <2020h> <'a' 'b'> <00h 'c'> <0040h> <0040h> <0010h> a = SP Card Status. '0'-No Card, '2'-Dual SP, '4'-Quad SP b = Linear Card Status. "0"-Not Installled, "1"-Installed c = Version Number (1.50 or higher) <0040h> <0040h> = 64 Register Writes, 64 Register Reads (Max.) <0010h> = 16 Register GUID/Scratch``` |
| 1101-1116 | GUID/Scratch | N/A | N/A | N/A | Read/Write | Reserved (may be used in future RLC software) |
| FACTORY SERVICE |  |  |  |  |  |  |
| 1151-1156 | Factory Service Registers | N/A | N/A | N/A | Read/Write | Factory Use Only - Do Not Modify |
| Math / Logic |  |  |  |  |  |  |
| 1121-1200 | Reserved for Math/Logic Operations |  |  |  |  |  |


| REGISTER ADDRESS | REGISTER NAME | LOW <br> LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ALARM PARAMETERS |  |  |  |  |  |  |
| Alarm 1 |  |  |  |  |  |  |
| 1201 | Assign | 0 | 1* | 1 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1202 | Action | 0 | 9 | 1 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\mathrm{bdIn}, 9=\mathrm{HCur} \end{aligned}$ |
| 1203 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1204 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1205 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1206 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1207 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1208 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1=\mathrm{Yes}$ |
| 1209 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| Alarm $2 \times 10$ |  |  |  |  |  |  |
| 1221 | Assign | 0 | 1* | 1 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1222 | Action | 0 | 9 | 1 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\text { bdIn, } 9=\mathrm{HCur} \end{aligned}$ |
| 1223 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1224 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1225 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1226 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1227 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1228 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1$ = Yes |
| 1229 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| Alarm 3 |  |  |  |  |  |  |
| 1241 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1242 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\mathrm{NONE}, 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\mathrm{bdIn}, 9=\mathrm{HCur} \end{aligned}$ |
| 1243 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1244 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1245 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1246 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1247 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1248 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1$ = Yes |
| 1249 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| Alarm 4 |  |  |  |  |  |  |
| 1261 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1262 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\mathrm{NONE}, 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\mathrm{bdIn}, 9=\mathrm{HCur} \end{aligned}$ |
| 1263 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1264 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 =0.1 Second |
| 1265 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1266 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1267 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1268 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1$ = Yes |
| 1269 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| Alarm 5 |  |  |  |  |  |  |
| 1281 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1282 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\text { bANd, } 8=\text { bdIn, } 9=\mathrm{HCur} \end{aligned}$ |
| 1283 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1284 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 =0.1 Second |
| 1285 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |


| REGISTER ADDRESS | REGISTER NAME | LOW LIMIT | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1286 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1287 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1288 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1=\mathrm{Yes}$ |
| 1289 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | $0=$ Off, 1 = On (Applies for TC or RTD input) |
| Alarm 6 |  |  |  |  |  |  |
| 1301 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, $2+$ = FlexCard Assignments |
| 1302 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\text { bdIn, } 9=\text { HCur } \end{aligned}$ |
| 1303 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1304 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1305 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1306 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1307 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1308 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1=\mathrm{Yes}$ |
| 1309 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | $0=$ Off, 1 = On (Applies for TC or RTD input) |
| Alarm 7 |  |  |  |  |  |  |
| 1321 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, $2+$ = FlexCard Assignments |
| 1322 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\mathrm{bdIn}, 9=\mathrm{HCur} \end{aligned}$ |
| 1323 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1324 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1325 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1326 | Output Logic | 0 | 1 | 0 | Read/Write | $0=$ Normal, 1 = Reverse |
| 1327 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1328 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1=\mathrm{Yes}$ |
| 1329 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | $0=$ Off, 1 = On (Applies for TC or RTD input) |
| Alarm 8 |  |  |  |  |  |  |
| 1341 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1342 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\text { bANd, } 8=\text { bdln, } 9=\text { HCur } \end{aligned}$ |
| 1343 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1344 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1345 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1346 | Output Logic | 0 | 1 | 0 | Read/Write | $0=$ Normal, 1 = Reverse |
| 1347 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1348 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1=\mathrm{Yes}$ |
| 1349 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | $0=$ Off, 1 = On (Applies for TC or RTD input) |
| Alarm 9 |  |  |  |  |  |  |
| 1361 | Assign | 0 | 1* | 0 | Read/Write | $0=$ NONE, 1 = PV, $2+$ = FlexCard Assignments |
| 1362 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\mathrm{bdln}, 9=\mathrm{HCur} \end{aligned}$ |
| 1363 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1364 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 =0.1 Second |
| 1365 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1366 | Output Logic | 0 | 1 | 0 | Read/Write | $0=$ Normal, 1 = Reverse |
| 1367 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1368 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1=\mathrm{Yes}$ |
| 1369 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | $0=$ Off, 1 = On (Applies for TC or RTD input) |
| Alarm 10 |  |  |  |  |  |  |
| 1381 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1382 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\text { bANd, } 8=\text { bdln, } 9=\text { HCur } \end{aligned}$ |


| REGISTER ADDRESS | REGISTER NAME | LOW <br> LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1383 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1384 | On Time Delay | 0 | 9999 | 0 | Read/Write | $1=0.1$ Second |
| 1385 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1386 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1387 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1388 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1=\mathrm{Yes}$ |
| 1389 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| Alarm 11 |  |  |  |  |  |  |
| 1401 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1402 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\mathrm{NONE}, 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\mathrm{bdIn}, 9=\mathrm{HCur} \end{aligned}$ |
| 1403 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1404 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1405 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1406 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1407 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1408 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1$ = Yes |
| 1409 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| Alarm 12 |  |  |  |  |  |  |
| 1421 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1422 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\text { bANd, } 8=\text { bdIn, } 9=\text { HCur } \end{aligned}$ |
| 1423 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1424 | On Time Delay | 0 | 9999 | 0 | Read/Write | $1=0.1$ Second |
| 1425 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1426 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1427 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1428 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1$ = Yes |
| 1429 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| Alarm 13 |  |  |  |  |  |  |
| 1441 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1442 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\text { bANd, } 8=\text { bdIn, } 9=\text { HCur } \end{aligned}$ |
| 1443 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1444 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1445 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1446 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1447 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1448 | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1$ = Yes |
| 1449 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| Alarm 14 |  |  |  |  |  |  |
| 1461 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1462 | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\text { bANd, } 8=\text { bdIn, } 9=\text { HCur } \end{aligned}$ |
| 1463 | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1464 | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 =0.1 Second |
| 1465 | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1466 | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1467 | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1468 | Standby Operation | 0 | 1 | 0 | Read/Write | 0 = No, 1 = Yes |
| 1469 | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |


| $\begin{aligned} & \hline \text { REGI } \\ & \text { ADD } \end{aligned}$ | $\begin{aligned} & \text { STER } \\ & \text { ESSS } \end{aligned}$ | REGISTER NAME | LOW LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Alarm 15 |  |  |  |  |  |  |  |
| 1481 |  | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1482 |  | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\mathrm{NONE}, 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\mathrm{bdIn}, 9=\mathrm{HCur} \end{aligned}$ |
| 1483 |  | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1484 |  | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1485 |  | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1486 |  | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1487 |  | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1488 |  | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1$ = Yes |
| 1489 |  | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| Alarm 16 |  |  |  |  |  |  |  |
| 1501 |  | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = PV, 2+ = FlexCard Assignments |
| 1502 |  | Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\text { NONE, } 1=\mathrm{AbHI}, 2=\mathrm{AbLO}, 3=\mathrm{AUHI}, 4=\mathrm{AULO}, 5=\mathrm{dEHI}, 6=\mathrm{dELO}, \\ & 7=\mathrm{bANd}, 8=\mathrm{bdIn}, 9=\mathrm{HCur} \end{aligned}$ |
| 1503 |  | Hysteresis Value | 1 | 9999 | 2 | Read/Write | 1 = 1 Display Unit |
| 1504 |  | On Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1505 |  | Off Time Delay | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Second |
| 1506 |  | Output Logic | 0 | 1 | 0 | Read/Write | 0 = Normal, 1 = Reverse |
| 1507 |  | Reset Action | 0 | 2 | 0 | Read/Write | 0 = Auto, 1 = Latch1, 2 = Latch2 |
| 1508 |  | Standby Operation | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1$ = Yes |
| 1509 |  | Probe Failure Action (TC or RTD Only) | 0 | 1 | 0 | Read/Write | 0 = Off, 1 = On (Applies for TC or RTD input) |
| ALARM SCALING PARAMETERS |  |  |  |  |  |  |  |
| List A | List B | Alarm Values |  |  |  |  |  |
| 1551 | 1651 | Alarm 1 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1552 | 1652 | Alarm 2 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1553 | 1653 | Alarm 3 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1554 | 1654 | Alarm 4 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1555 | 1655 | Alarm 5 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1556 | 1656 | Alarm 6 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1557 | 1657 | Alarm 7 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1558 | 1658 | Alarm 8 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1559 | 1659 | Alarm 9 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1560 | 1660 | Alarm 10 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1561 | 1661 | Alarm 11 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1562 | 1662 | Alarm 12 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1563 | 1663 | Alarm 13 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1564 | 1664 | Alarm 14 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1565 | 1665 | Alarm 15 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1566 | 1666 | Alarm 16 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 1567 | 1667 | Alarm 1 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1568 | 1668 | Alarm 2 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1569 | 1669 | Alarm 3 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1570 | 1670 | Alarm 4 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1571 | 1671 | Alarm 5 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1572 | 1672 | Alarm 6 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1573 | 1673 | Alarm 7 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1574 | 1674 | Alarm 8 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1575 | 1675 | Alarm 9 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1576 | 1676 | Alarm 10 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1577 | 1677 | Alarm 11 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |


| REGISTER ADDRESS |  | REGISTER NAME | $\begin{aligned} & \hline \text { LOW } \\ & \text { LIMIT } \end{aligned}$ | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1578 | 1678 | Alarm 12 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1579 | 1679 | Alarm 13 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1580 | 1680 | Alarm 14 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1581 | 1681 | Alarm 15 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| 1582 | 1682 | Alarm 16 Band/Dev. Value | -1999 | 9999 | 0 | Read/Write | Applicable only for Band or Deviation Alarm Action. 1 = 1 Display Unit |
| SERIAL COMMUNICATION PARAMETERS |  |  |  |  |  |  |  |
| 1701 |  | USB Mode | 0 | 1 | 0 | Read/Write | 0 = Configuration, 1 = Serial |
| 1702 |  | Type | 0 | 2 | 2 | Read/Write | $0=$ RLC Protocol (ASCII), 1 = Modbus RTU, $2=$ Modbus ASCII |
| 1703 |  | Baud Rate | 0 | 5 | 5 | Read/Write | $\begin{aligned} & 0=1200,1=2400,2=4800,3=9600,4=19200, \\ & 5=38400 \end{aligned}$ |
| 1704 |  | Data Bits | 0 | 1 | 1 | Read/Write | $0=7$ Bits, 1 = 8 Bits |
| 1705 |  | Parity | 0 | 2 | 0 | Read/Write | 0 = None, 1 = Even, 2 = Odd |
| 1706 |  |  | 0 | 99 | 0 | Read/Write | RLC Protocol: 0-99 |
|  |  | Address | 1 | 247 | 247 |  | Modbus: 1-247 |
| 1707 |  | Transmit Delay | 0 | 250 | 10 | Read/Write | $1=0.001$ Second |
| 1708 |  | Abbreviated Transmission (RLC only) | 0 | 1 | 0 | Read/Write | $0=$ No, $1=$ Yes (Not used when communications type is Modbus) |
| 1709 |  | Print Options (RLC only) | 0 | 8191 | 1 | Read/Write | $0=$ No, $1=$ Yes (Not used when communications type is Modbus) Bit $0-$ Print Input Value, Bit 1 - Print SP Value, Bit 2 - Print Setpoint Ramp Rate, Bit 3 - Print Output Power, Bit 4 - Print Proportional Value, Bit 5 - Print Integral Value, Bit 6 - Print Derivative Value, Bit 7 - Print Alarm Status, Bit 8 - Print Alarm 1 Value, Bit 9 - Print Alarm 2 Value, Bit 10 - Print Alarm 3 Value, Bit 11 - Print Alarm 4 Value, Bit 12 - Print Control Status Bits |
| 1710 |  | Load Serial Settings | 0 | 1 | 0 | Read/Write | Changing 41701-41710 will not update the PAX2C until this register is written with a 1 . After the write, the communicating device must be changed to new PAX2C settings and this register returns to 0 . |
| PROFILE CONTROL |  |  |  |  |  |  |  |
| 5001 |  | Profile 1 Cycle Count | 1 | 250 | 1 | Read/Write | 1-249 = Number of times to run profile, $250=$ Run Profile continuously |
| 5002 |  | Profile 1 Link to Profile | 0 | 16 | 0 | Read/Write | $0=$ No; 1-16 = Profile 1 to 16 |
| 5003 |  | Profile 1 Deviation Error Value | 0 | 9999 | 50 | Read/Write | $1=1$ process unit |
| 5004 |  | Profile 1 Error Time | 0 | 9999 | 0 | Read/Write | $1=0.1$ Minute |
| 5005 |  | Profile 1 Power Cycle Status | 0 | 2 | 0 | Read/Write | $0=$ End per PEnd, 1 = Cont (Continue /Resume), 2 = Strt (Start) |
| 5006 |  | Profile 1 PS2 SP Assignment | 0 | $0^{*}$ | 0 | Read/Write | 0 = NONE; $1+=$ FlexCard PID (Pid) |
| 5007 |  | Profile 1 PS2 Process Deviation Error Value | 0 | 9999 | 50 | Read/Write | $1=1$ process unit |
| 5008 |  | Profile 1 PID Select | 0 | 8 | 0 | Read/Write | $0=$ NO; $1=$ PS1 $\ldots .6=$ PS6, $7=$ SPSL, $8=$ Auto |
| 5009 |  | Profile 1 End Action | 0 | 9 | 0 | Read/Write | $\begin{aligned} & 0=\mathrm{End}, 1=\mathrm{StOP}, 2=\mathrm{OFF}, 3=\mathrm{SP} 1,4=\mathrm{SP} 2,5=\mathrm{SP} 3,6=\mathrm{SP} 4,7=\mathrm{SP} 5, \\ & 8=\mathrm{SP6}, 9=\mathrm{SPu} \end{aligned}$ |
| 5010 |  | Profile 1 End Segment | 1 | 20 | 20 | Read/Write | Last Segment to be used |
| 5011 |  | Profile 1 Last Profile | 0 | 1 | 0 | Read/Write | 0 = NO (read only); 1 = yES |
|  |  |  |  |  |  |  |  |
| 5021 |  | Profile 2 Registers |  |  |  |  | See Profile 1 |
| 5041 |  | Profile 3 Registers |  |  |  |  | See Profile 1 |
| 5061 |  | Profile 4 Registers |  |  |  |  | See Profile 1 |
| 5081 |  | Profile 5 Registers |  |  |  |  | See Profile 1 |
| 5101 |  | Profile 6 Registers |  |  |  |  | See Profile 1 |
| 5121 |  | Profile 7 Registers |  |  |  |  | See Profile 1 |
| 5141 |  | Profile 8 Registers |  |  |  |  | See Profile 1 |
| 5161 |  | Profile 9 Registers |  |  |  |  | See Profile 1 |
| 5181 |  | Profile 10 Registers |  |  |  |  | See Profile 1 |
| 5201 |  | Profile 11 Registers |  |  |  |  | See Profile 1 |
| 5221 |  | Profile 12 Registers |  |  |  |  | See Profile 1 |
| 5241 |  | Profile 13 Registers |  |  |  |  | See Profile 1 |


| REGISTER ADDRESS | REGISTER NAME | LOW <br> LIMIT | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 5261 | Profile 14 Registers |  |  |  |  | See Profile 1 |
| 5281 | Profile 15 Registers |  |  |  |  | See Profile 1 |
| 5301 | Profile 16 Registers |  |  |  |  | See Profile 1 |
| Profile Segment Registers |  |  |  |  |  | To calculate specific register number of Segment y, for Profile $x$ use formula: Profile $x$ Segment y register $=6000+(x-1)^{*} 100+(y-1) 5+$ Offset |
| 6001 | Profile 1 Segment Registers |  |  |  |  |  |
| 6101 | Profile 2 Segment Registers |  |  |  |  |  |
| 6201 | Profile 3 Segment Registers |  |  |  |  |  |
| 6301 | Profile 4 Segment Registers |  |  |  |  |  |
| 6401 | Profile 5 Segment Registers |  |  |  |  |  |
| 6501 | Profile 6 Segment Registers |  |  |  |  |  |
| 6601 | Profile 7 Segment Registers |  |  |  |  |  |
| 6701 | Profile 8 Segment Registers |  |  |  |  |  |
| 6801 | Profile 9 Segment Registers |  |  |  |  |  |
| 6901 | Profile 10 Segment Registers |  |  |  |  |  |
| 7001 | Profile 11 Segment Registers |  |  |  |  |  |
| 7101 | Profile 12 Segment Registers |  |  |  |  |  |
| 7201 | Profile 13 Segment Registers |  |  |  |  |  |
| 7301 | Profile 14 Segment Registers |  |  |  |  |  |
| 7401 | Profile 15 Segment Registers |  |  |  |  |  |
| 7501 | Profile 16 Segment Registers |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  | Offset |  |  |  |  |  |
| 1 | Profile ( $x+1$ ) PS1 Setpoint Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 process unit; Limited by Setpoint Limit Low and Setpoint Limit High |
| 2 | Profile ( $x+1$ ) PS2 Setpoint Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 process unit; Limited by Setpoint Limit Low and Setpoint Limit High |
| 3 | Profile ( $x+1$ ) Time Value/Ramp Rate | 0 | 9999 | 0 | Read/Write | 1 = 0.1 minute or 1 = 1 PV Display Unit/Min (when Ramp/Rate) |
| 4 | Profile ( $x+1$ ) Mode Register | 0 | 0 | 4032 (0xFC0) | Read/Write | Bit 11: Event Flag 4 State; $1=0 N, 0=O F F$ <br> Bit 10: Event Flag 3 State; $1=\mathrm{ON}, 0=\mathrm{OFF}$ <br> Bit 9: Event Flag 2 State; $1=\mathrm{ON}, 0=\mathrm{OFF}$ <br> Bit 8: Event Flag 1 State; $1=\mathrm{ON}, 0=\mathrm{OFF}$ <br> Bit 7: $1=0.1 \mathrm{Min}$; $0=1 \mathrm{Min}$ <br> Bit 6: 1 = Start Point Adjust; $0=$ Start Point Adjust disabled <br> Bit 5: <br> Bit 4: 1 = Use Ramp Rate (Reg 3 is Ramp Rate); $0=$ Reg 3 is Time Value <br> Bit 3: 1 = Error Delay when PS2 PV is above ScSP + Sc Error Value <br> Bit 2: 1 = Error Delay when PS2 PV is below ScSP - Sc Error Value <br> Bit 1: 1 = Error when PV above SP + Er-V <br> Bit 0: 1 = Error when PV below SP - Er-V |

* Higher limit is applicable with FlexCard installed.

| REGISTER ADDRESS: | REGISTER NAME | $\begin{aligned} & \hline \text { LOW } \\ & \text { LIMIT } \end{aligned}$ | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FREQUENTLY USED REGISTERS |  |  |  |  |  |  |
| 4n001 | Input Process Value (Hi word) | -1999 | 9999 |  | Read Only | 1 = 1 Display Unit <br> ADC Overrange Value $=1048576$, Underrange Value $=-1048576$ |
| 4n002 | Input Process Value (Lo word) |  |  |  |  |  |
| 4 n 003 | Input Process Maximum (Hi word) | -1999 | 9999 | N/A | Read Only | 1 = 1 Display Unit |
| 4n004 | Input Process Maximum (Lo word) |  |  |  |  |  |
| 4n005 | Input Process Minimum (Hi word) | -1999 | 9999 | N/A | Read Only | 1 = 1 Display Unit |
| 4n006 | Input Process Minimum (Lo word) |  |  |  |  |  |
| 4n007 | Active SP | -1999 | 9999 | N/A | Read/Write | 1 = 1 Display Unit |
| 4n008 | Active Remote SP | -1999 | 9999 | N/A | Read Only | 1 = 1 Display Unit |
| 4n009 | Status Flags | 0 | 255 | N/A | Read Only | Bit 8 Set = ADC Underrange, <br> Bit 7 Set = ADC Overrange. <br> Bit 6 Set = SP Ramping <br> Bit 5 Set $=$ Auto Tune Fail <br> Bit 4 Set = Auto Tune Done <br> Bit 3:0 = Auto Tune Phase |
| 4n010 | Output Status Register | 0 | 15 | 0 | Read/Write | Status of Solid-State Outputs. Bit State: $0=$ OFF, $1=0 N$. Bit $3=04$, Bit $2=03$, Bit $1=02$, Bit $0=01$. |
| 4n011 | Heat Power | 0 | 1000 | 0 | Read Only | 1 $=0.1 \%$ |
| $4 \mathrm{n012}$ | Cool Power | 0 | 1000 | 0 | Read Only | 1=0.1\% |
| 4 n 013 | Integral Sum |  |  |  | Read Only |  |
| 4 n 014 | Active Proportional Band | 0 | 9999 | 700 | Read/Write | 1 = 1 display unit |
| 4 n 015 | Active Integral Time | 0 | 65000 | 120 | Read/Write | 1 = 0.1 Second |
| 4 n 016 | Active Derivative Time | 0 | 9999 | 30 | Read/Write | $1=0.1$ Second |
| 4 n 017 | Active Power Filter | 0 | 60 | 10 | Read/Write | $1=0.1$ Second |
| 4 n 018 | Heat Gain | 0 | 5000 | 1000 | Read/Write | 1 = 0.1\% |
| 4n019 | Cool Gain | 0 | 5000 | 1000 | Read/Write | 1 = 0.1\% |
| 4n020-4n024 | Reserved |  |  |  |  |  |
| 4n035 | PID Control Flags | 0 | 1000 | 0 | Read/Write | Bit 9: Stop PID; 0=No, 1=Yes (Px2C V2+) <br> Bit 6-8: AutoTune; $0=$ No, $1=$ Yes, $2=$ CS1 $. . .7=$ CS6 <br> Bit 6: AutoTune; $0=$ NO, $1=\mathrm{YES}$ <br> Bit 5: MAN; $0=$ PID Auto Mode, 1 = PID Manual (User) Mode; <br> Bit 4: PSEL; $0=$ PS1 PID, 1 = Alternate PID, <br> Bit 3: ILOC; $0=$ Enable Integral Action, 1 = Disable Integral Action; <br> Bit 2: RSPt; $0=$ Local SP, $1=$ Remote SP; <br> Bit 1: SPSL; $0=$ SP1, $1=$ Req. SP2; <br> Bit 0: SPrP; $0=$ SP Ramping Enable, $1=$ SP Ramping Disable |
| 4n041 | Control Flags 2 | 0 | 118 | 0 | Read/Write | Bit 4-6: PSEL; 0 = PS1 ... 5 = PS6, 6 = SPSL, 7 = Auto (PX2C V2+) Bit 0-2: SPSL; $0=$ SP1 $\ldots 5=$ SP6, $6=$ SPu (Px2C Ver 2+) |
| INPUT PARAMETERS |  |  |  |  |  | SEE INPUT MODULE FOR PARAMETER DESCRIPTIONS |
| Analog Input Parameters |  |  |  |  |  |  |
| 4n071 | Input Type | 0 | 1 | 0 | Read/Write | $0=0$ to 10 V DC, $1=0$ to 20 mA DC |
| 4n072 | Input Square Root Linearization | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1=\mathrm{Yes}$ |
| 4n073 | Input Decimal Point | 0 | 3 | 3 | Read/Write | $0=0,1=0.0,2=0.00,3=0.000$ |
| 4 n 074 | Input Rounding | 0 | 6 | 0 | Read/Write | $0=1,1=2,2=5,3=10,4=20,5=50,6=100$ |
| 4 n 075 | Input Offset Value (Hi word) | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 4n076 | Input Offset Value (Lo word) |  |  |  |  |  |
| 4 n 077 | Input Filter Value | 0 | 250 | 10 | Read/Write | 1 = 0.1 Second |


*: $\mathrm{n}=1$ + FlexCard Address


## *: n = 1 + FlexCard Address

- PAX2 Unit and FlexCard dependent

| REGISTER ADDRESS : | REGISTER NAME | LOW LIMIT | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 4n255 | Output 2 Assignment | 0 | - | 0 | Read/Write | Same as Output 1 Assignment |
| 4n256 | Output 2 Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 4n257 | Output 2 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Output 1 Alarm Mask |
| 4n258 | Output 2 Cycle Time | 0 | 600 | 20 | Read/Write | 1 = 0.1 Second |
| 4n259 | Output 3 Assignment | 0 | * | 0 | Read/Write | Same as Output 1 Assignment |
| 4n260 | Output 3 Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 4n261 | Output 3 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Output 1 Alarm Mask |
| 4n262 | Output 3 Cycle Time | 0 | 600 | 20 | Read/Write | 1 = 0.1 Second |
| 4n263 | Output 4 Assignment | 0 | * | 0 | Read/Write | Same as Output 1 Assignment |
| 4n264 | Output 4 Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |
| 4n265 | Output 4 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Output 1 Alarm Mask |
| 4n266 | Output 4 Cycle Time | 0 | 600 | 20 | Read/Write | 1 = 0.1 Second |
| PID CONFIGURATION PARAMETERS |  |  |  |  |  |  |
| Control Parameters |  |  |  |  |  |  |
| 4n301 | Assign | 0 | 1* | 0 | Read/Write | 0 = NONE, 1 = P2C Process Value, 2+ = Flex Card Assignments; FCn Input |
| 4n302 | Control Type | 0 | 2 | 0 | Read/Write | 0 = Heat, 1 = Cool, 2 = Both |
| 4n303 | Control Mode | 0 | 1 | 0 | Read/Write | 0 = Automatic, 1 = Manual |
| 4n304 | Manual Power | -1999 | 2000 | 0 | Read/Write | Output Power: Heat/Cool; $1=0.1 \%$; *-writeable only in manual mode |
| Remote Setpoint Parameters |  |  |  |  |  |  |
| 4n306 | Remote SP Assignment | 0 | 1* | 0 | Read/Write | $0 \text { = NONE, } 1 \text { = P2C SP, } 2 \text { = P2C PV, } 3 \text { = P2C OP, } 4 \text { = P2C ScSP, 5+ = Flex }$ Card Assignments ; FCn SP, FCn PV, FCn OP |
| 4n307 | Reserved Register | -32768 | -32768 | N/A |  |  |
| 4n308 | Ratio | 1 | 9999 | 1000 | Read/Write | $1=0.1$ |
| 4n309 | Bias | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 4n310 | Select Local / Remote SP | 0 | 1 | 0 | Read/Write |  |
| Setpoint Parameters |  |  |  |  |  |  |
| 4n311 | Setpoint Selection | 0 | 1 | 0 | Read/Write | 0 = Setpoint 1, 1 = Setpoint 2 |
| 4n312 | Sepoint 1 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 4n313 | Setpoint 2 Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 4n314 | Setpoint Lo Limit Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 4n315 | Setpoint Hi Limit Value | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |
| 4n316 | Ramp Timebase | 0 | 3 | 0 | Read/Write | 0 = Off, 1 = Seconds, 2 = Minutes, 3 = Hours |
| 4n317 | Ramp Rate | 0 | 9999 | 0 | Read/Write | 1 = 0.1 Ramp Timebase unit |
| PID Parameters |  |  |  |  |  |  |
| 4n321 | PID Parameter Selection | 0 | 1 | 0 | Read/Write | 0 = PS1, 1 = PS2, 2 = PS3, 3 = PS4, 4 = PS5, 5 = PS6, 6 = SPSL, 7 = Auto |
| 4n322 | PS1 Proportional Band | 0 | 9999 | 40 | Read/Write | 1 = 1 Display Unit |
| 4n323 | PS1 Integral Time | 0 | 65000 | 120 | Read/Write | 1 = 0.1 Second |
| 4n324 | PS1 Derivative Time | 0 | 9999 | 30 | Read/Write | 1 = 0.1 Second |
| 4n325 | PS1 Power Filter Value | 0 | 600 | 10 | Read/Write | 1 = 0.1 Second |
| 4n326 | PS1 Output Power Offset | -1000 | 1000 | 0 | Read/Write | 1 = 0.1 \%; Applicable when PS1 Integral Time is 0 |
| 4n327 | PS2 Proportional Band | 0 | 9999 | 40 | Read/Write | 1 = 1 Display Unit |
| 4n328 | PS2 Integral Time | 0 | 65000 | 120 | Read/Write | 1 = 0.1 Second |
| 4n329 | PS2 Derivative Time | 0 | 9999 | 30 | Read/Write | $1=0.1$ Second |
| 4n330 | PS2 Power Filter Value | 0 | 600 | 10 | Read/Write | $1=0.1$ Second |
| 4n331 | PS2 Output Power Offset | -1000 | 1000 | 0 | Read/Write | 1 = 0.1 \%; Applicable when PS2 Integral Time is 0 |
| Power Transfer Parameters |  |  |  |  |  |  |
| 4n341 | Input Fault Power Value | -1999 | 2000 | 0 | Read/Write | 1 = 0.1 \% |
| 4n342 | Output Deadband | -1000 | 1000 | 0 | Read/Write | 1 = 0.1 \% |
| 4n343 | Output Heat Gain | 0 | 5000 | 1000 | Read/Write | 1 = 0.1 \% |

*: $\mathrm{n}=1$ + FlexCard Address

- PAX2 Unit and FlexCard dependent


[^0]** - See Modbus Table for PAX2 unit (FlexBus model) in which card is being installe

| REGISTER ADDRESS : | REGISTER NAME | LOW LIMIT | HIGH <br> LIMIT | FACTORY SETTING | ACCESS | COMMENTS |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FREQUENTLY USED REGISTERS |  |  |  |  |  |  |  |  |  |  |
| 4n001 | Input Process Value (Hi word) | -1999 | 9999 | N/A | Read Only | 1 = 1 Display Unit ADC Overrange Value $=1048576$, Underrange Value $=-1048576$ |  |  |  |  |
| 4n002 | Input Process Value (Lo word) |  |  |  |  |  |  |  |  |  |
| 4n003 | Input Process Maximum (Hi word) | -1999 | 9999 | N/A | Read Only | 1 = 1 Display Unit |  |  |  |  |
| 4n004 | Input Process Maximum (Lo word) |  |  |  |  |  |  |  |  |  |
| 4n005 | Input Process Minimum (Hi word) | -1999 | 9999 | N/A | Read Only | 1 = 1 Display Unit |  |  |  |  |
| 4n006 | Input Process Minimum (Lo word) |  |  |  |  |  |  |  |  |  |
| 4n007 | Input Process Status Flags | 0 | 255 | N/A | Read Only | Bit 3 Set = ADC Underrange, Bit 2 Set = ADC Overrange . |  |  |  |  |
| 4n008 | Output Status Register | 0 | 15 | 0 | Read/Write | Status of Solid-State Outputs. Bit State: 0=OFF, 1=ON. <br> Bit $3=04$, Bit $2=03$, Bit $1=02$, Bit $0=01$ <br> * only outputs configured for ASGN=NONE are writeable; otherwise writes are ignored |  |  |  |  |
| INPUT PARAMETERS |  |  |  |  |  | SEE INPUT MODULE FOR PARAMETER DESCRIPTIONS |  |  |  |  |
| Analog Input Parameters |  |  |  |  |  |  |  |  |  |  |
| 4n071 | Heater Current Monitor | 0 | 4* | 1 | Read/Write | 0 = None, 1 = P2C Out1, 2 = P2C Out2, 3 = P2C Out3, 4=P2C Out4, 5+ = FlexCard Outputs |  |  |  |  |
| 4n072 | Input Square Root Linearization | 0 | 1 | 0 | Read/Write | $0=\mathrm{No}, 1$ = Yes |  |  |  |  |
| 4n073 | Input Decimal Point | 0 | 3 | 1 | Read/Write | $0=0,1=0.0,2=0.00,3=0.000$ |  |  |  |  |
| 4n074 | Input Rounding | 0 | 6 | 0 | Read/Write | $0=1,1=2,2=5,3=10,4=20,5=50,6=100$ |  |  |  |  |
| 4n075 | Input Offset Value (Hi word) | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |  |  |  |  |
| 4n076 | Input Offset Value (Lo word) |  |  |  |  |  |  |  |  |  |
| 4n077 | Input Filter Value | 0 | 250 | 10 | Read/Write | 1 = 0.1 Second |  |  |  |  |
| 4n078 | Input Filter Band Value | 0 | 250 | 10 | Read/Write | 1 = 1 display unit |  |  |  |  |
| 4n079 | Max (HI) Capture Delay Time | 0 | 9999 | 0 | Read/Write | 0 = Max Update Rate, $1=0.1 \mathrm{Sec}$ |  |  |  |  |
| 4n080 | Min (LO) Capture Delay Time | 0 | 9999 | 0 | Read/Write | 0 = Max Update Rate, $1=0.1 \mathrm{Sec}$ |  |  |  |  |
| 4n081 | Display Input Units | 0 | 1 | 0 | Read/Write | 0 = OFF, 1 = ON |  |  |  |  |
| 4n082 | Input Units Character 1 | 0 | 57 | 0 | Read/Write | Label Mnemonic Characters <br> $0=$ $9=\mathrm{I}$ $18=\mathrm{Q}$ <br> $1=\mathrm{A}$ $10=\mathrm{J}$ $19=\mathrm{R}$ <br> $2=\mathrm{b}$ $11=\mathrm{K}$ $20=\mathrm{S}$ <br> $3=\mathrm{C}$ $12=\mathrm{L}$ $21=\mathrm{t}$ <br> $4=\mathrm{d}$ $13=\mathrm{M}(\mathrm{l})$ $22=\mathrm{U}$ <br> $5=\mathrm{E}$ $14=\mathrm{M}(\mathrm{r})$ $23=\mathrm{V}$ <br> $6=\mathrm{F}$ $15=\mathrm{N}$ $24=\mathrm{W}(\mathrm{I})$ <br> $7=\mathrm{G}$ $16=\mathrm{O}$ $25=\mathrm{W}(\mathrm{r})$ <br> $8=\mathrm{H}$ $17=\mathrm{P}$ $26=\mathrm{Y}$ | $\begin{aligned} & 27=Z \\ & 28=0 \\ & 29=1 \\ & 30=2 \\ & 31=3 \\ & 32=4 \\ & 33=5 \\ & 34=6 \\ & 35=7 \end{aligned}$ | $\begin{aligned} & 36=8 \\ & 37=9 \\ & 38=\mathrm{a} \\ & 39=\mathrm{c} \\ & 40=\mathrm{e} \\ & 41=\mathrm{g} \\ & 42=\mathrm{h} \\ & 43=\mathrm{i} \\ & 44=\mathrm{n} \end{aligned}$ | $\begin{aligned} & 45=m(r) \\ & 46=o \\ & 47=q \\ & 48=r \\ & 49=u \\ & 50=w(r) \\ & 51=- \\ & 52== \\ & 53=[ \end{aligned}$ | $\begin{aligned} & 54=] \\ & 55=1 \\ & 56=0 \\ & 57= \end{aligned}$ |
| 4n083 | Input Units Character 2 | 0 | 57 | 0 | Read/Write | See Input Units Character 1 |  |  |  |  |
| 4n084 | Input Units Character 3 0 57 0 Read/Write |  |  |  |  | See Input Units Character 1 |  |  |  |  |
| Input Scaling Point Parameters |  |  |  |  |  |  |  |  |  |  |
| 4n101 | Number of Scaling Points | 2 | 15 | 2 | Read/Write | Number of Linearization Scaling Points |  |  |  |  |
| 4n102 | Reserved | N/A | N/A | N/A | N/A | Reserved for future use |  |  |  |  |
| 4n103 | Scaling Pt. 1 Input Value (Hi word) | 0 | 9999 | 0 | Read/Write | $1=0.001$ |  |  |  |  |
| 4n104 | Scaling Pt. 1 Input Value (Lo word) |  |  |  |  |  |  |  |  |  |
| 4n105 | Scaling Pt. 1 Display Value (Hi word) | -1999 | 9999 | 0 | Read/Write | 1 = 1 Display Unit |  |  |  |  |
| 4n106 | Scaling Pt. 1 Display Value (Lo word) |  |  |  |  |  |  |  |  |  |
| 4n107 | Scaling Pt. 2 Input Value (Hi word) | 0 | 9999 | 1000 | Read/Write | $1=0.001$ |  |  |  |  |
| 4n108 | Scaling Pt. 2 Input Value (Lo word) |  |  |  |  |  |  |  |  |  |
| 4n109 | Scaling Pt. 2 Display Value (Hi word) | -1999 | 9999 | 1000 | Read/Write | 1 = 1 Display Unit |  |  |  |  |
| 4n110 | Scaling Pt. 2 Display Value (Lo word) |  |  |  |  |  |  |  |  |  |

[^1]| REGISTER ADDRESS: | REGISTER NAME | LOW LIMIT | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { 4n111 } \\ \text { thru } 4 n 162 \end{gathered}$ | Scaling Pts. 3 thru 15 Values | $\begin{array}{\|c\|} \hline 0 \text { (input) } \\ -1999 \text { (dsp) } \\ \hline \end{array}$ | 9999 | 0 | Read/Write | Registers 40111-40162 hold values for Scaling Points 3 thru 15, and follow the same ordering as Scaling Points 1 and 2. |  |  |  |
| DISPLAY CONFIGURATION PARAMETERS |  |  |  |  |  |  |  |  |  |
| Line 2 Input LOCS Parameters |  |  |  |  |  |  |  |  |  |
| 4n201 | Line 2 Input (PV) Display Access | 0 | 21 | 0 | Read/Write | 0 = LOC; Bit 0 = drEd, Bit $2=$ PrEd, Bit4 = HrEd; Other bits N/A |  |  |  |
| 4n202 | Line 2 Maximum (Hi) Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit } 4=\text { HrEd, Bit5 }=\text { HEnt } \end{aligned}$ |  |  |  |
| 4 n 203 | Line 2 Minimum (Lo) Value Access | 0 | 42 | 0 | Read/Write | $\begin{aligned} & 0=\text { LOC; Bit } 0=\text { drEd, Bit } 1=\text { dEnt, Bit } 2=\text { PrEd, Bit } 3=\text { PEnt, } \\ & \text { Bit4 }=\text { HrEd, Bit5 }=\text { HEnt } \end{aligned}$ |  |  |  |
| Line 2 Function LOCS Parameters |  |  |  |  |  |  |  |  |  |
| 4n231 | Line 2 Reset Max Display Access | 0 | 42 | 0 | Read/Write | 0 = LOC; Bit 1 = dEnt, Bit $3=$ PEnt, Bit5 $=$ HEnt; Other bits N/A |  |  |  |
| 4n232 | Line 2 Reset Min Display Access | 0 | 42 | 0 | Read/Write | $0=$ LOC; Bit $1=\mathrm{dEnt}$, Bit $3=$ PEnt, Bit5 $=$ HEnt; Other bits N/A |  |  |  |
| 4n233 | Line 2 Reset Max and Min Access | 0 | 42 | 0 | Read/Write | 0 = LOC; Bit 1 = dEnt, Bit 3 = PEnt, Bit5 = HEnt; Other bits N/A |  |  |  |
| Hardware Label Mnemonic |  |  |  |  |  | Replaces "FCx" in main, parameter, and hidden display loops when programmed |  |  |  |
| 4 n 246 | Hardware Label Character 1 | 0 | 57 | 0 | Read/Write | $\|$Label Mnemonic Characters   <br> $0=$ $9=\mathrm{I}$ $18=\mathrm{Q}$ $27=\mathrm{Z}$ <br> $1=\mathrm{A}$ $10=\mathrm{J}$ $19=\mathrm{R}$ $28=0$ <br> $2=\mathrm{b}$ $11=\mathrm{K}$ $20=\mathrm{S}$ $29=1$ <br> $3=\mathrm{C}$ $12=\mathrm{L}$ $21=\mathrm{t}$ $30=2$ <br> $4=\mathrm{C}$ $13=\mathrm{M}(\mathrm{I})$ $22=\mathrm{U}$ $31=3$ <br> $5=\mathrm{E}$ $14=\mathrm{M}(\mathrm{r})$ $23=\mathrm{V}$ $32=4$ <br> $6=\mathrm{F}$ $15=\mathrm{N}$ $24=\mathrm{W}(\mathrm{l})$ $33=5$ <br> $7=\mathrm{G}$ $16=\mathrm{O}$ $25=\mathrm{W}(\mathrm{r})$ $34=6$ <br> $8=\mathrm{H}$ $17=\mathrm{P}$ $26=\mathrm{Y}$ $35=7$ | $\begin{aligned} & 36=8 \\ & 37=9 \\ & 38=\mathrm{a} \\ & 39=\mathrm{c} \\ & 40=\mathrm{e} \\ & 41=\mathrm{g} \\ & 42=\mathrm{h} \\ & 43=\mathrm{i} \\ & 44=\mathrm{n} \end{aligned}$ | $\begin{aligned} & 45=m(r) \\ & 46=0 \\ & 47=q \\ & 48=r \\ & 49=u \\ & 50=w(r) \\ & 51=- \\ & 52== \\ & 53=[ \end{aligned}$ | $\begin{aligned} & 54=] \\ & 55=1 \\ & 56=0 \\ & 57= \end{aligned}$ |
| 4n247 | Hardware Label Character 2 | 0 | 57 | 0 | Read/Write | See Hardware Label Character 1 |  |  |  |
| 4n248 | Hardware Label Character 3 | 0 | 57 | 0 | Read/Write | See Hardware Label Character 1 |  |  |  |
| OUTPUT PARAMETERS |  |  |  |  |  |  |  |  |  |
| 4n251 | Output 1 Assignment | 0 | PAX2 Unit and FlexCard dependent | 0 | Read/Write | Assignments dependent on PAX2 model in which FlexCard is installed. Output Assignment List order = PX2, FC1, FC2, FC3 <br> Number of PX2FCA1 Output Assignments $=0$ |  |  |  |
| 4n252 | Output 1 Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, 2 = OR |  |  |  |
| 4n253 | Output 1 Alarm Mask | 0 | 65535 | 0 | Read/Write | Bit $0=$ A1 Bit $4=$ A5 Bit $8=$ A9 Bit $12=$ A13 <br> Bit $1=$ A2 Bit $5=$ A6 Bit $9=$ A10 Bit 13 $=$ A14 <br> Bit 2 A Bit $6=$ A7 Bit 10 $=$ A11 Bit 14 $=$ A15 <br> Bit 3 A4 Bit $7=$ A8 Bit 11 $=$ A12 Bit 15 $=$ A16 |  |  |  |
| 4 n 254 | Output 1 Cycle Time | 0 | 600 | 20 | Read/Write | $1=0.1$ Second |  |  |  |
| 4 n 255 | Output 2 Assignment | 0 | 6 | 0 | Read/Write | Same as Output 1 Assignment |  |  |  |
| 4n256 | Output 2 Alarm Logic Mode | 0 | 2 | 0 | Read/Write | 0 = SINGLE, 1 = AND, $2=0 \mathrm{O}$ |  |  |  |
| 4 n 257 | Output 2 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Output 1 Alarm Mask |  |  |  |
| 4 n 258 | Output 2 Cycle Time | 0 | 600 | 20 | Read/Write | $1=0.1$ Second |  |  |  |
| 4n259 | Output 3 Assignment | 0 | 6 | 0 | Read/Write | Same as Output 1 Assignment |  |  |  |
| 4n260 | Output 3 Alarm Logic Mode | 0 | 2 | 0 | Read/Write | $0=$ SINGLE, 1 = AND, $2=0 \mathrm{O}$ |  |  |  |
| 4n261 | Output 3 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Output 1 Alarm Mask |  |  |  |
| 4n262 | Output 3 Cycle Time | 0 | 600 | 20 | Read/Write | 1 = 0.1 Second |  |  |  |
| 4n263 | Output 4 Assignment | 0 | 6 | 0 | Read/Write | Same as Output 1 Assignment |  |  |  |
| 4n264 | Output 4 Alarm Logic Mode | 0 | 2 | 0 | Read/Write | $0=$ SINGLE, 1 = AND, $2=0 \mathrm{O}$ |  |  |  |
| 4 n 265 | Output 4 Alarm Mask | 0 | 65535 | 0 | Read/Write | Same as Output 1 Alarm Mask |  |  |  |
| 4 n 266 | Output 4 Cycle Time | 0 | 600 | 20 | Read/Write | $1=0.1$ Second |  |  |  |


| REGISTER ADDRESS : | REGISTER NAME | $\begin{aligned} & \hline \text { LOW } \\ & \text { LIMIT } \end{aligned}$ | HIGH LIMIT | FACTORY SETTING | ACCESS | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PX2 USER INPUT / FUNCTION KEYS PARAMETERS |  |  |  | REFER TO PAX2 MANUAL FOR STARTING LOCATION OF FLEXCARD FUNCTIONS (NUMBER OF PAX2 FUNCTIONS + 1) |  |  |
| ** | User Input Selection | 0 | FlexCard Dependent | 0 | Read/Write | $n+1=d-H I$ $n+3=d-L O$ $n+5=r-H L$ <br> $n+2=r-H I$ $n+4=r-L o$ $n+6=N A-1$ <br> $\mathrm{n}=$ Starting location for Flex Card <br> Function List order = PAX2, FC1, FC2, FC3 <br> Number of PX2FCA01 User Functions $=6$ |
| ** | User Key Selection | 0 | FlexCard Dependent | 0 | Read/Write | $\begin{aligned} & \mathrm{n}+1=r-\mathrm{HI} \quad \mathrm{n}+2=r-\mathrm{Lo} \quad \mathrm{n}+3=r-\mathrm{HL} \quad \mathrm{n}+4=\text { NA-1 } \\ & \mathrm{n}=\text { Starting location for Flex Card } \\ & \text { Function List order = PAX2, FC1, FC2, FC3 } \\ & \text { Number of PX2FCA01 Key Functions }=4 \end{aligned}$ |

*: $\mathrm{n}=1$ + FlexCard Address
** - See Modbus Table for PAX2 unit (FlexBus model) in which card is being installed


[^0]:    *: $\mathrm{n}=1+$ FlexCard Address

[^1]:    *: n = 1 + FlexCard Address

